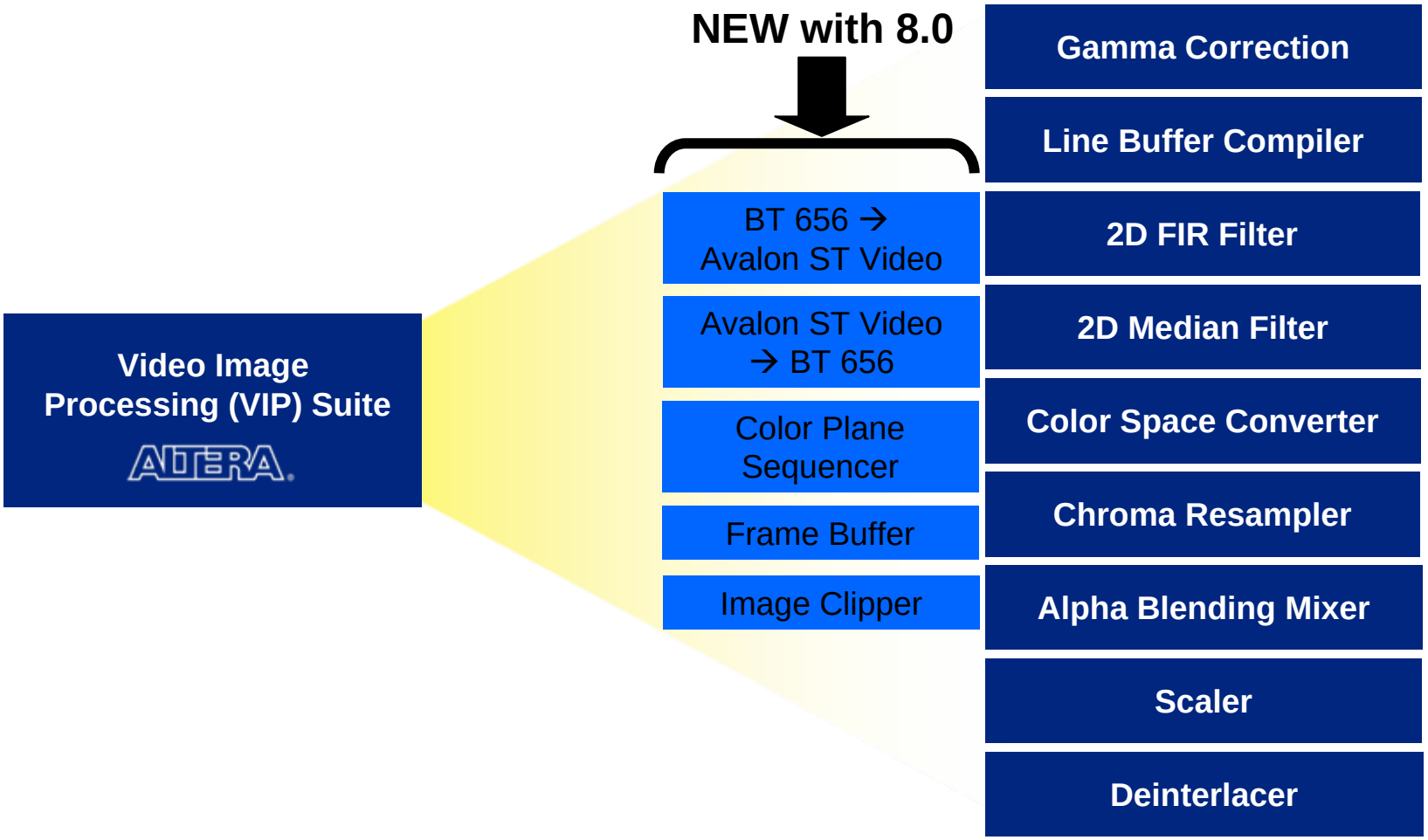
Altera Video Image Processing (VIP) Solution

Agenda

- What is the VIP Suite of intellectual property (IP) cores?
- Why we built VIP Suite: Typical signal chains implemented using VIP cores
- Overall VIP value proposition
- VIP Suite – core details
- Available VIP resources

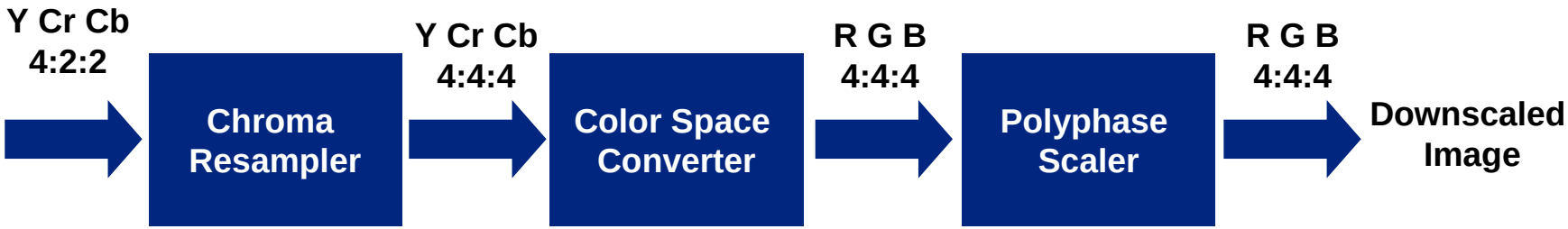
Video Image Processing (VIP)



Suite of building block IP for video processing

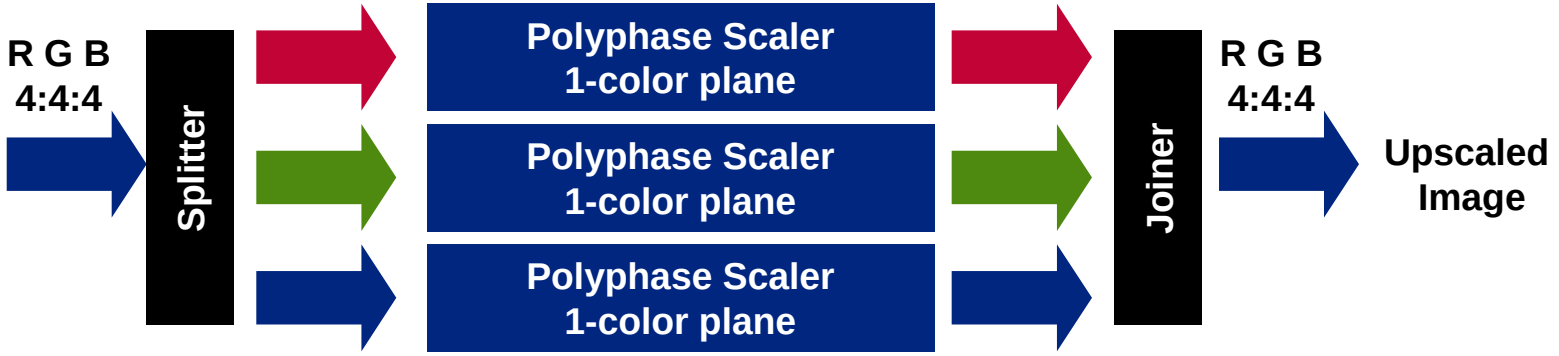
Downscaling – Monitoring Application

- In various kinds of systems, there is a need to downscale and view large video frames on a small display – monitoring signal chain
- VIP cores let you quickly build a high-quality monitoring signal chain by combining the polyphase scaler with other appropriate cores; an example is shown below



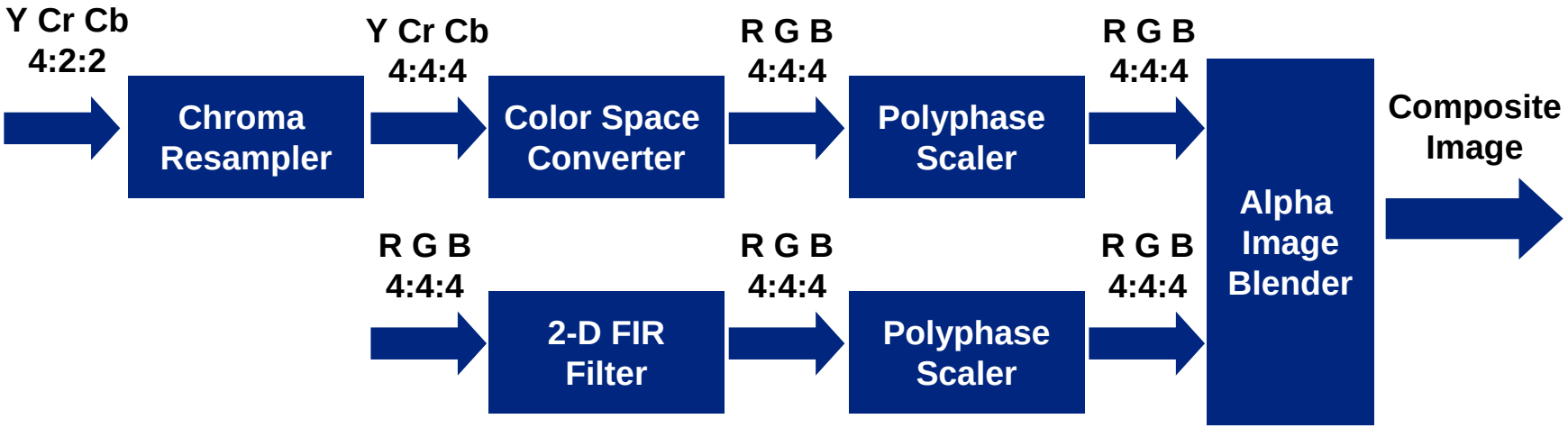
Upscaling – Zooming-In Application

- In various kinds of systems, there is a need to crop a certain section of a video frame and upscale that portion to view on a display
- VIP cores let you quickly build a high-quality upscaler using the built-in crop features within the scaler
- The bicubic scaling option that is built in the VIP scaler offers the best quality/resource trade-off for an upscaling application



Video Mixing Application

- In various kinds of systems, there is a need to mix two streams of video and display on the screen
- The VIP core can let you quickly build multiple custom video processing chains and mix, for example, two streams using the alpha blending core



Typical Signal Chains: Summary

- There are various other types of signal chains that can implemented using the VIP cores as well as using VIP cores in conjunction with your custom cores
- VIP cores are designed for easy connectivity, allowing you to start a design using a VIP core and swap it with your custom function
- In many applications the VIP cores are used to do the simple pre-processing and combined with your custom IP to create a complete signal chain

think AND not OR

Altera @ 40 nm

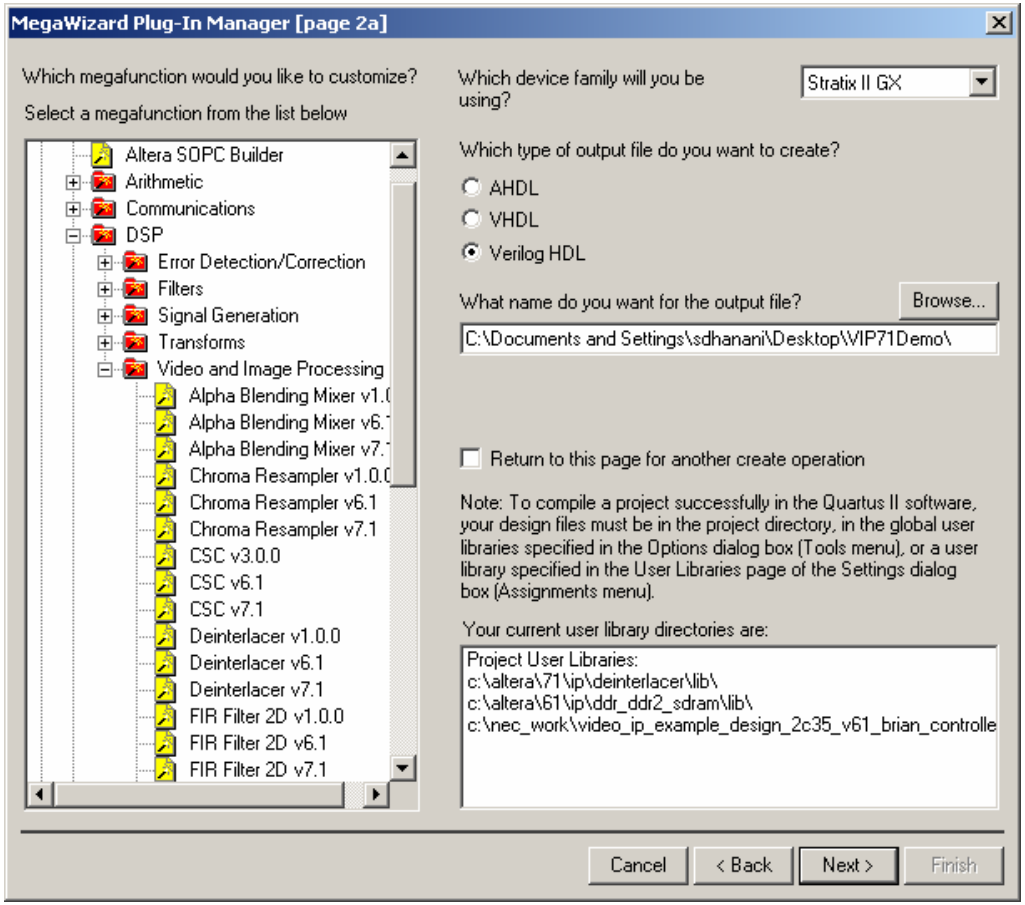
Overall VIP Value Proposition

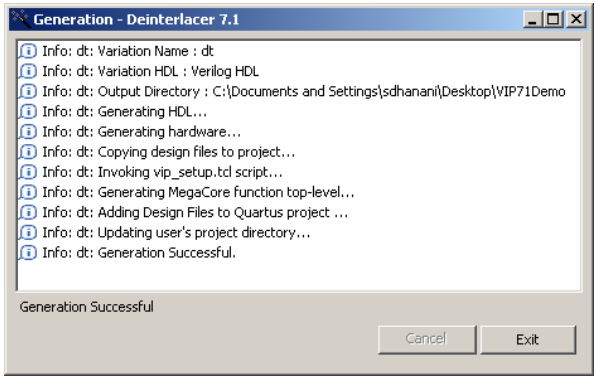
Video Image Processing with FPGAs

- Video processing that is ***computationally intensive***, fits elegantly in the inherently parallel FPGA architecture i.e.
  - Polyphase video scaling
  - Motion estimation/compensation
  - Motion adaptive deinterlacing
- VIP Suite consists of blocks commonly used to implement complex video/image processing circuits

Using Altera VIP Cores: Quartus II Software

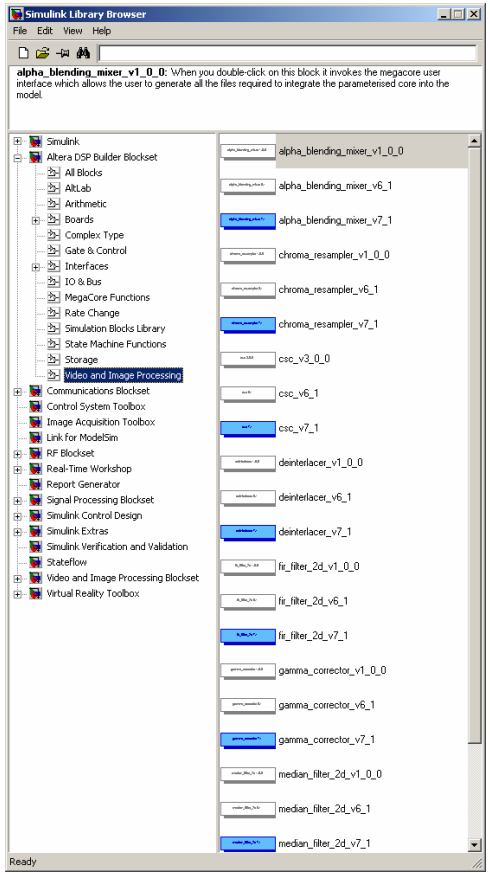
- VIP cores are configurable using Quartus® design software

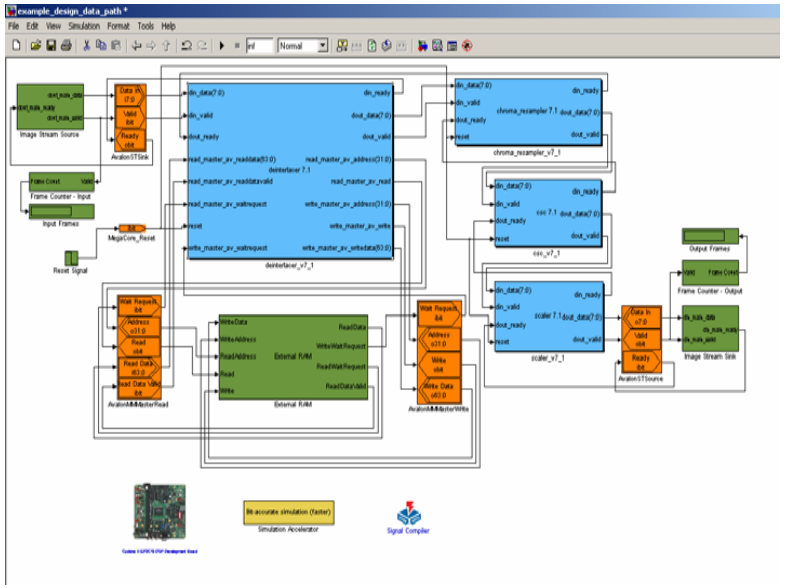




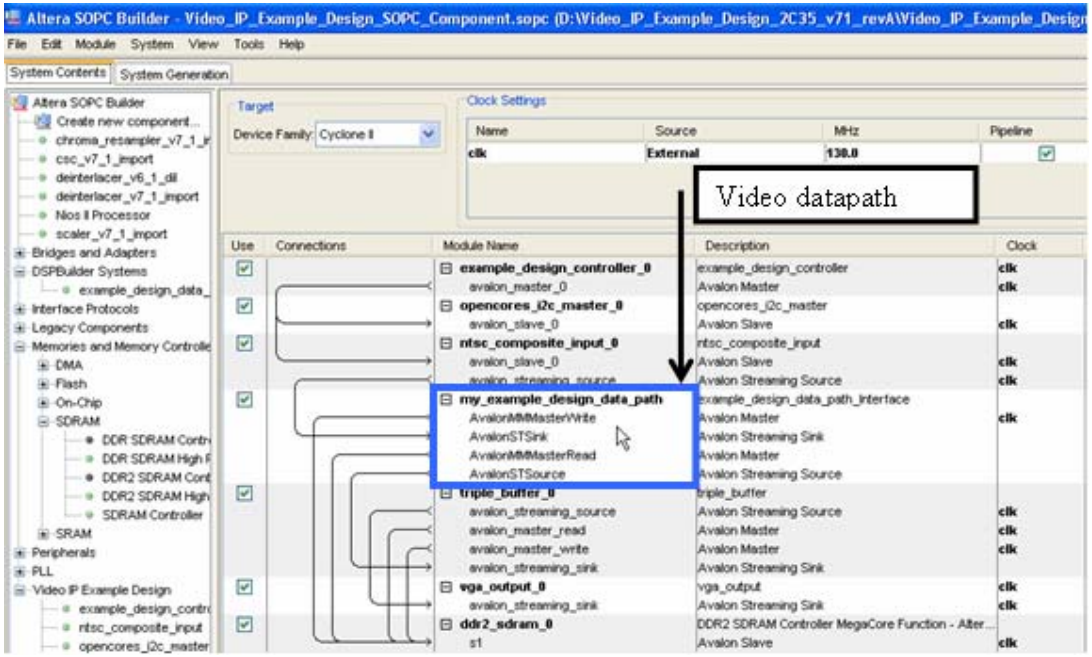
Using Altera VIP Cores: Simulink

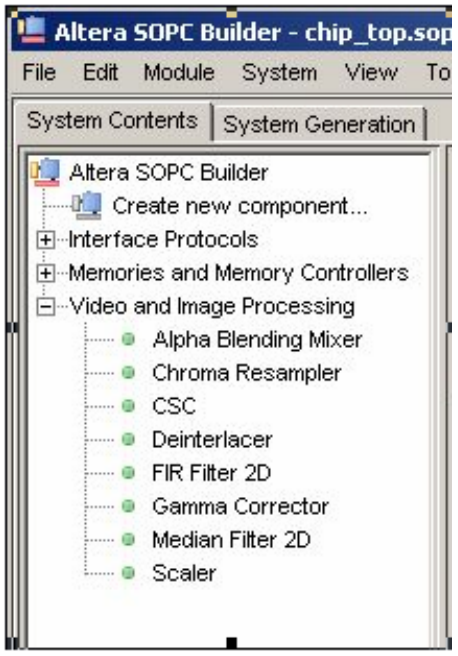
- VIP Suite can be configured using MATLAB/Simulink





SOPC Builder Support





- All the VIP cores are SOPC Builder ready – they can be instantiated and connected using the SOPC Builder environment
- VIP signal chain built and simulated using Simulink can also be exported as a system on a programmable chip (SOPC) component and connected to other system blocks using the SOPC Builder

VIP Value Proposition

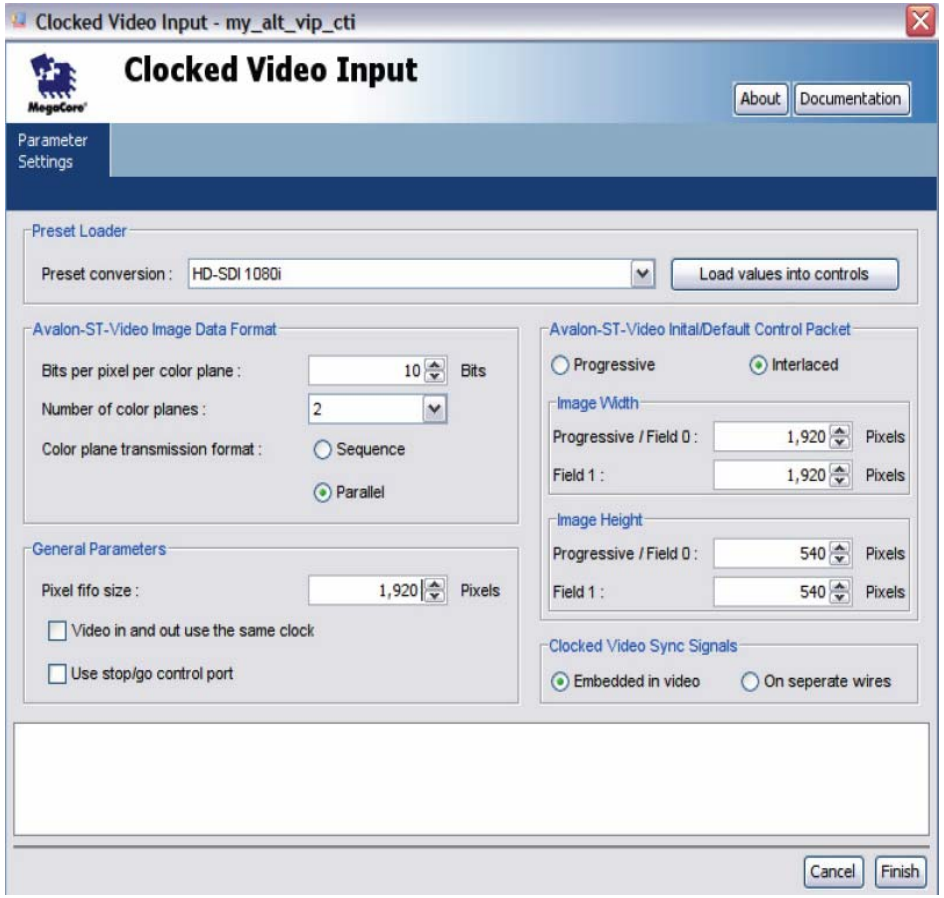
- Altera VIP Suite of cores are basic building blocks for video/imaging systems
- VIP IP cores speed up your development cycle by allowing you to focus on IP that is your value add
- VIP cores are designed for easy connectivity, enabling seamless mix-and-match of Altera and proprietary cores

Accelerating Your Time to Market

VIP Suite – Core Details

VIP Suite: Avalon ST Video → Clocked Video

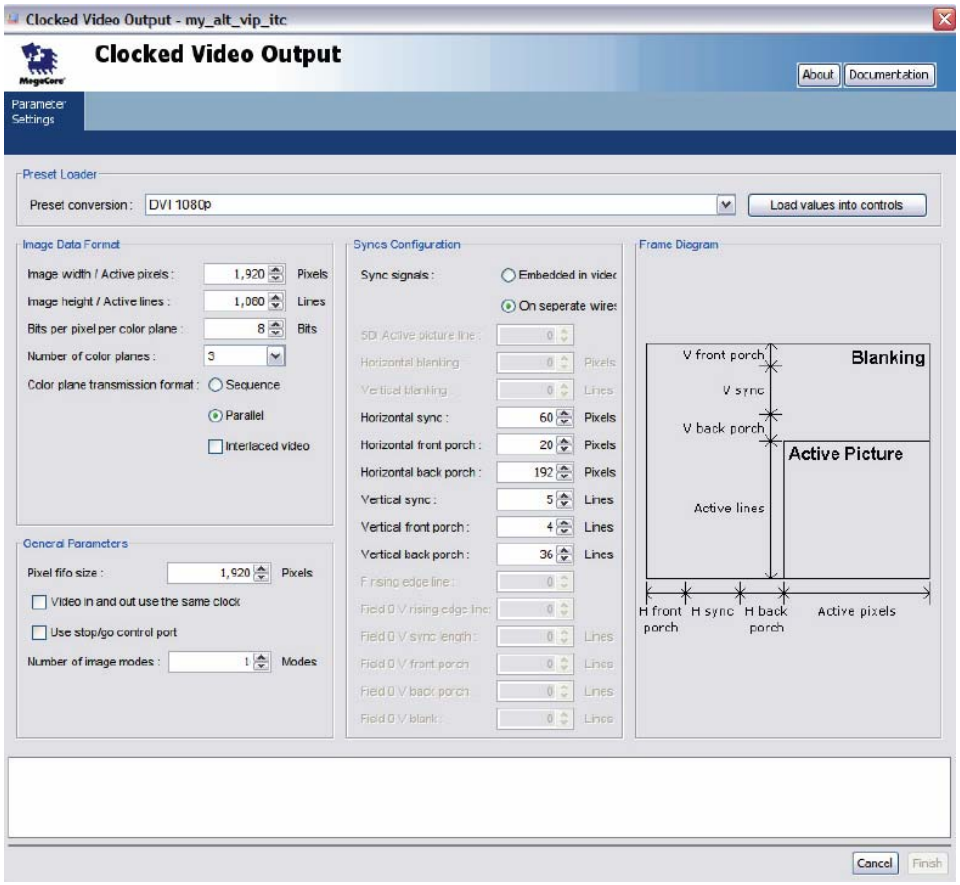
NEW with 8.0



- For example if the input is a HD-SDI 1080i video stream
  - Select that format in the pull down menu
  - Set other parameters such as bits per pixel, # of color planes, image dimensions, etc as shown
  - Automatically conver from SDI to Avalon ST Video format

VIP Suite: Clocked Video → Avalon ST Video

NEW with 8.0

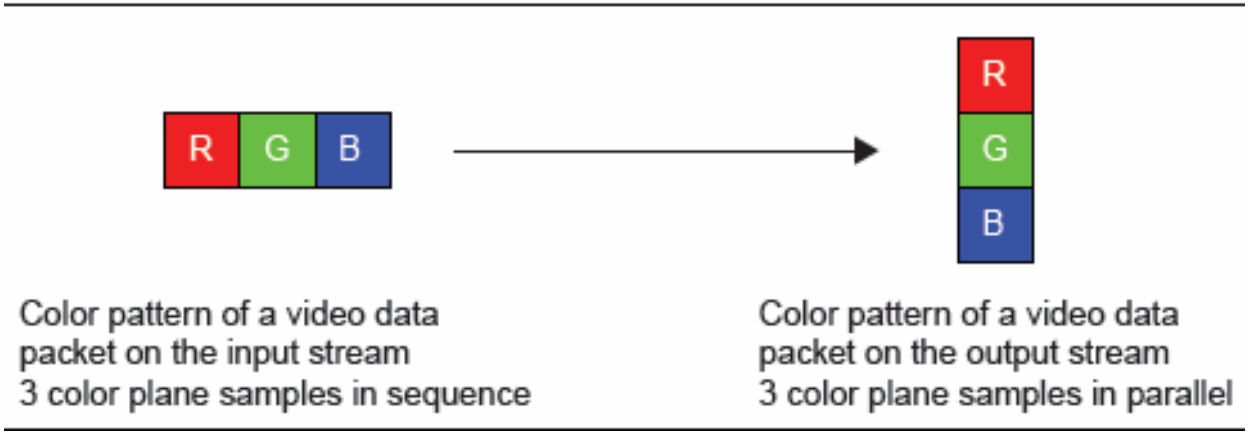


- For example if you need to create a DVI 1080p video stream
  - Select that format in the pull down menu
  - Set other parameters such as bits per pixel, # of color planes, image dimensions, etc as shown
  - Select the sync parameters
  - Automatically convert from Avalon ST Video to the DVI format

VIP Suite: Color Plane Sequencer

NEW with 8.0

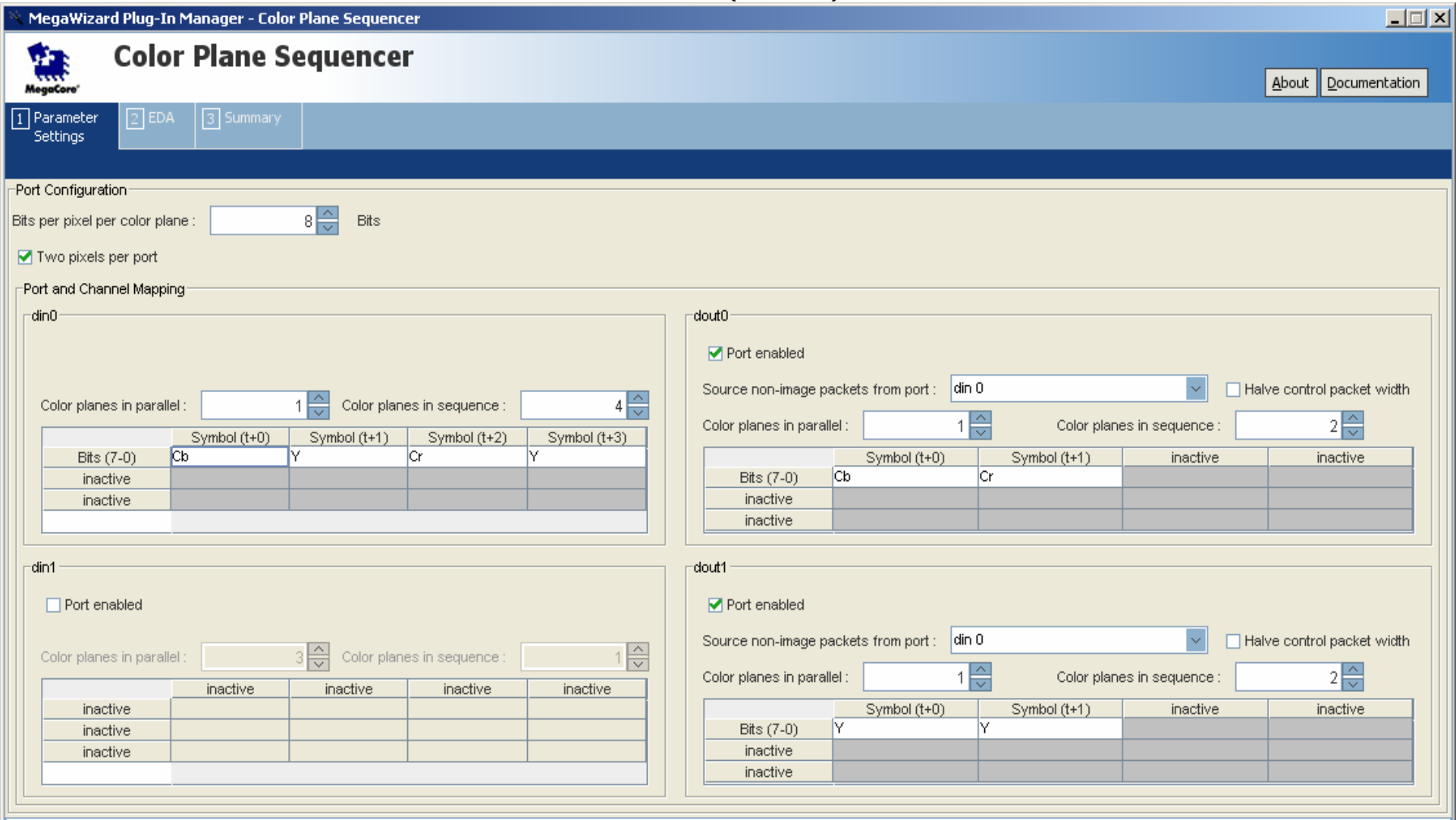
- The Color Plane Sequencer can change how color plane samples are transmitted across the Avalon-ST interface
- The color pattern of a video data packet can be rearranged in any valid combination of channels in sequence and parallel.
- The Color Plane Sequencer can also drop color planes.



VIP Suite: Color Plane Sequencer

NEW with 8.0

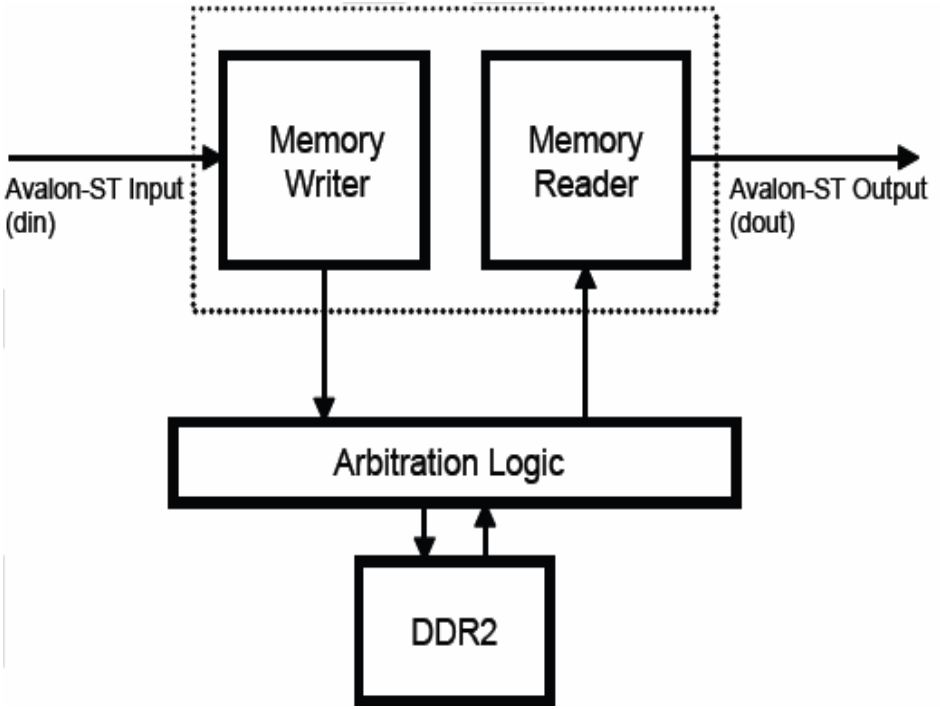
Example shows a Color Plane Sequencer used to split an Avalon-ST video containing 4:2:2 subsampled data (Y'CbCr) into separate luminance (Y') and chrominance (Cb,Cr) streams



VIP Suite: Frame Buffer

NEW with 8.0

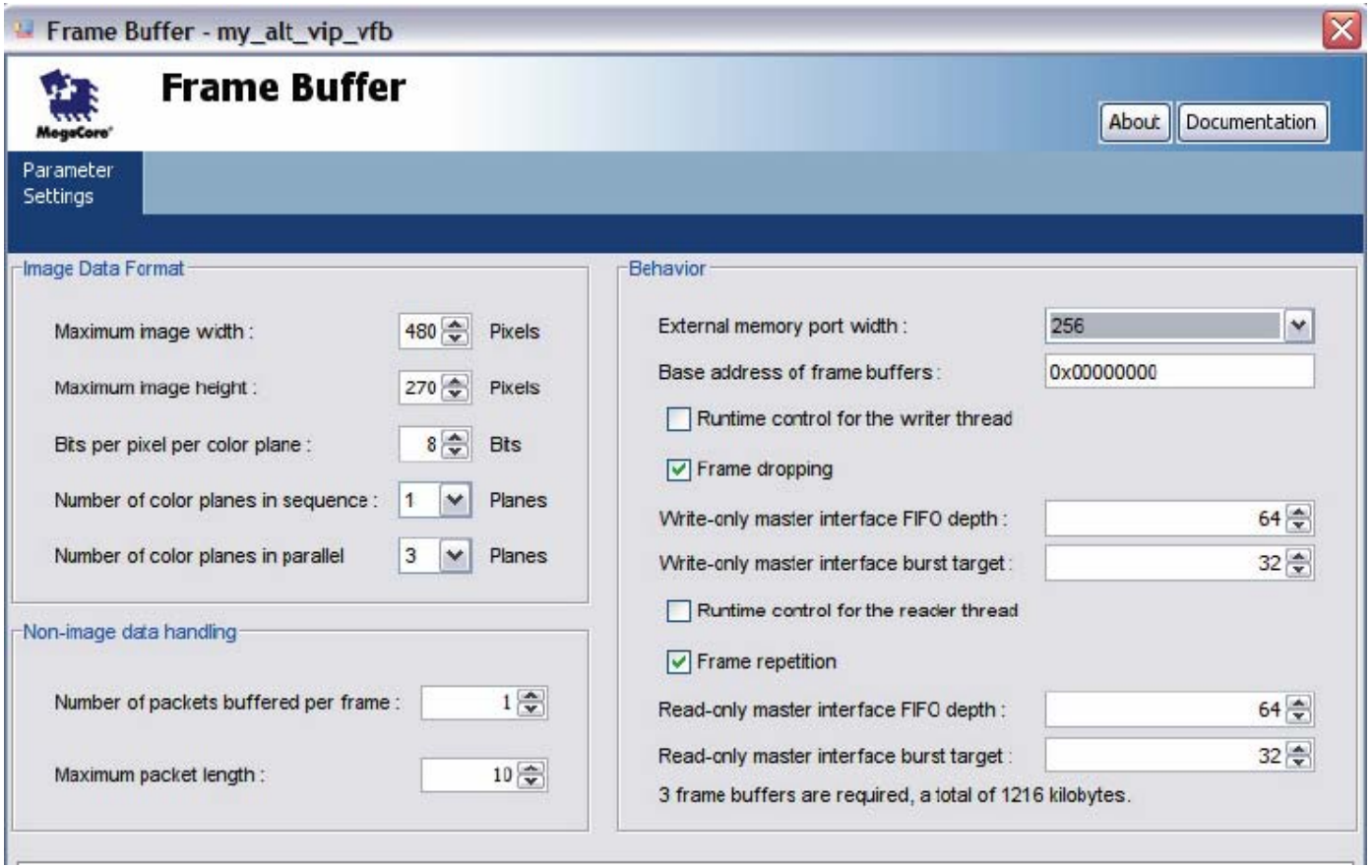
- The Frame Buffer core is used to buffer video frames into external RAM
- It supports double or triple-buffering with a range of options for frame dropping and repeating
- The Frame Buffer is built with two basic blocks
  - A writer which stores input pixels into memory
  - A reader which retrieves video frames from the memory and outputs them



VIP Suite: Frame Buffer

NEW with 8.0

- Frame Buffer settings to allow for triple-buffering of a 480×720 R'G'B' video stream transmitted in parallel



VIP Suite: Clipper

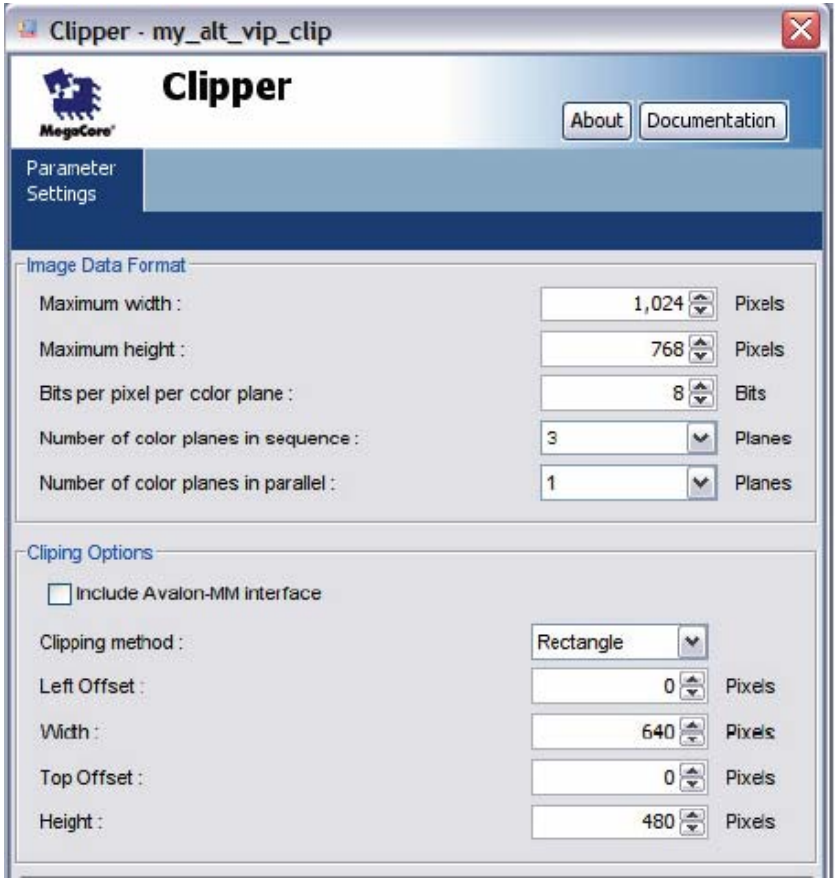
NEW with 8.0

- The Clipper MegaCore function provides a means to select an active area from a video stream and discard the remainder
- The active region can be specified by either providing the offsets from each border, or by providing a point to be the top-left corner of the active region along with the region's width and height
- The Clipper can deal with changing input resolutions by reading Avalon-ST Video control packets
- An optional Avalon-MM interface allows the clipping settings to be changed at runtime

VIP Suite: Clipper

NEW with 8.0

- Shown is a Clipper core parameterized to crop the upper-left 640×480 pixels of a 1024×768 video stream.



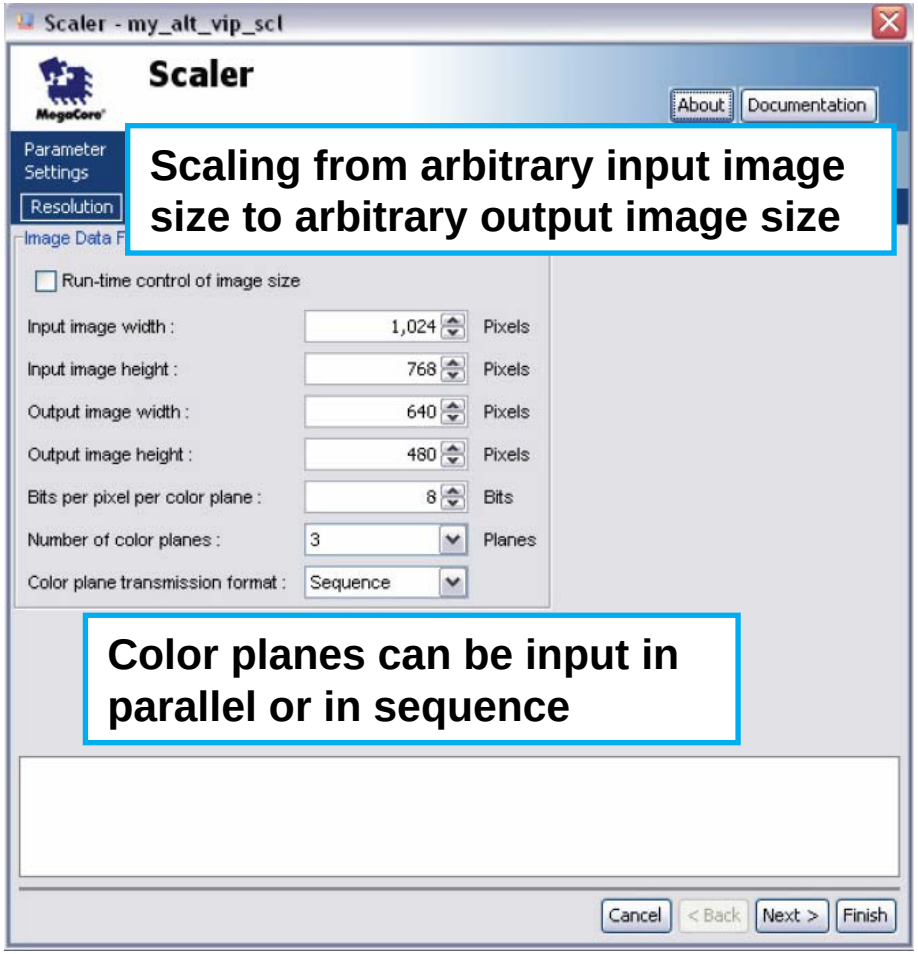
VIP Suite: Run-time Configurable Polyphase Scaling

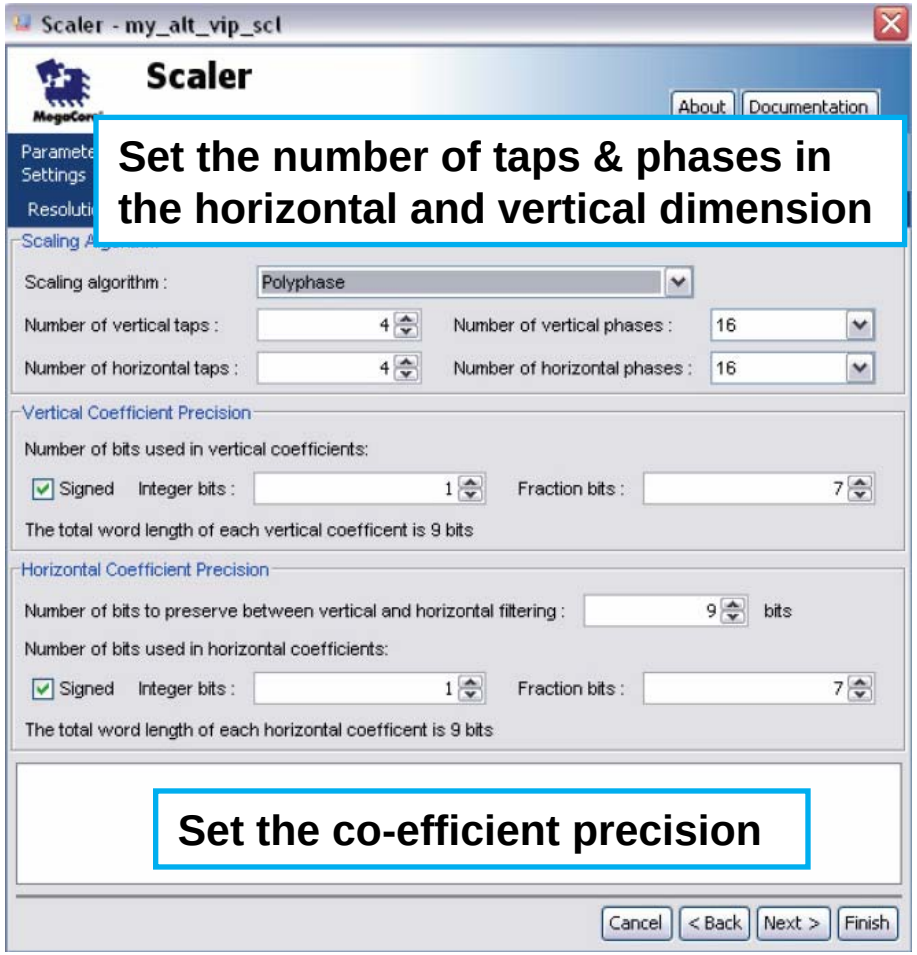
D1/SDTV: 720x480

HDTV 1080p: 1920x1080

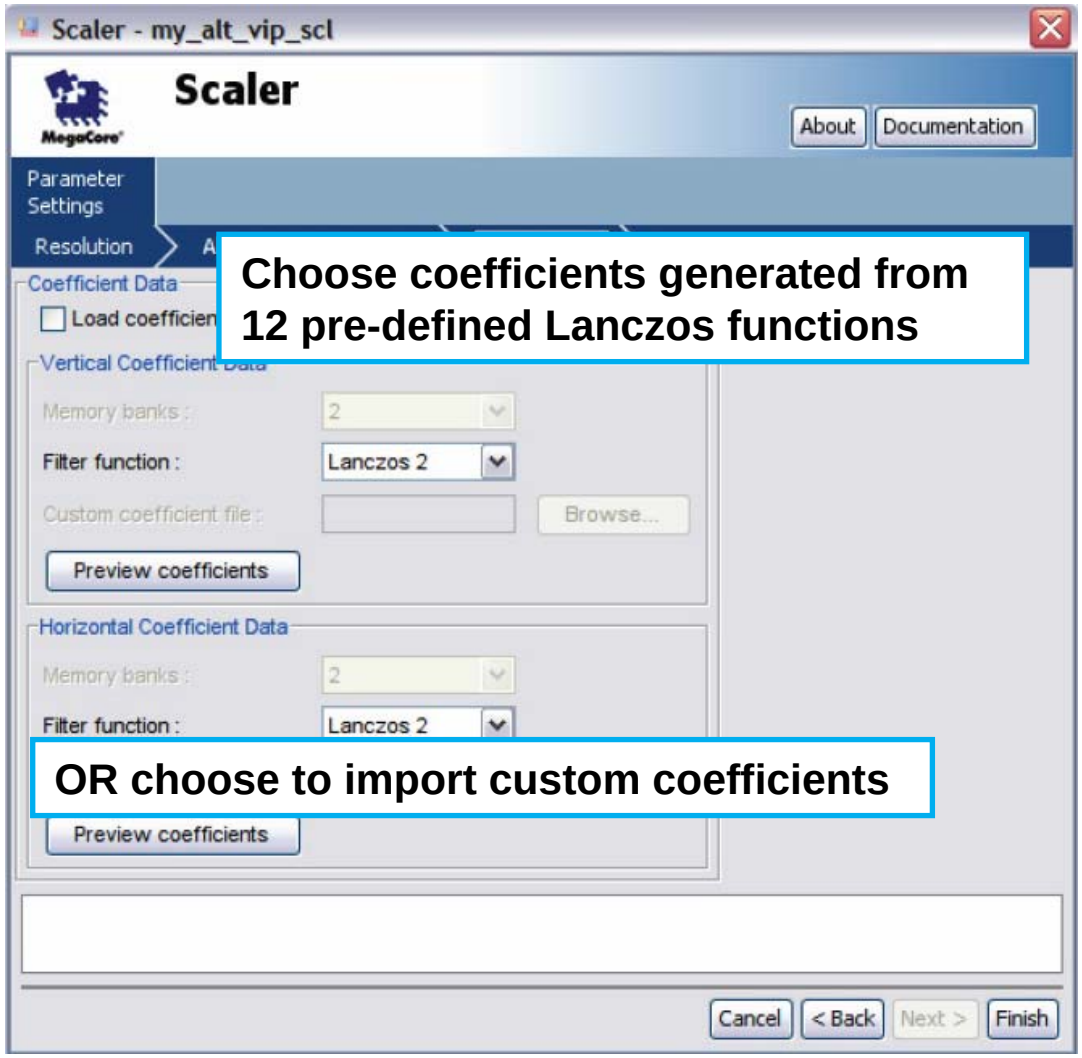
- High-quality multi-tap scaler with use models in monitoring (downscaling) and zooming (upscaling) applications

VIP Suite: Run-time Configurable Polyphase Scaling





VIP Suite: Run-time Configurable Polyphase Scaling



Choose coefficients generated from 12 pre-defined Lanczos functions

OR choose to import custom coefficients

Preview the coefficients

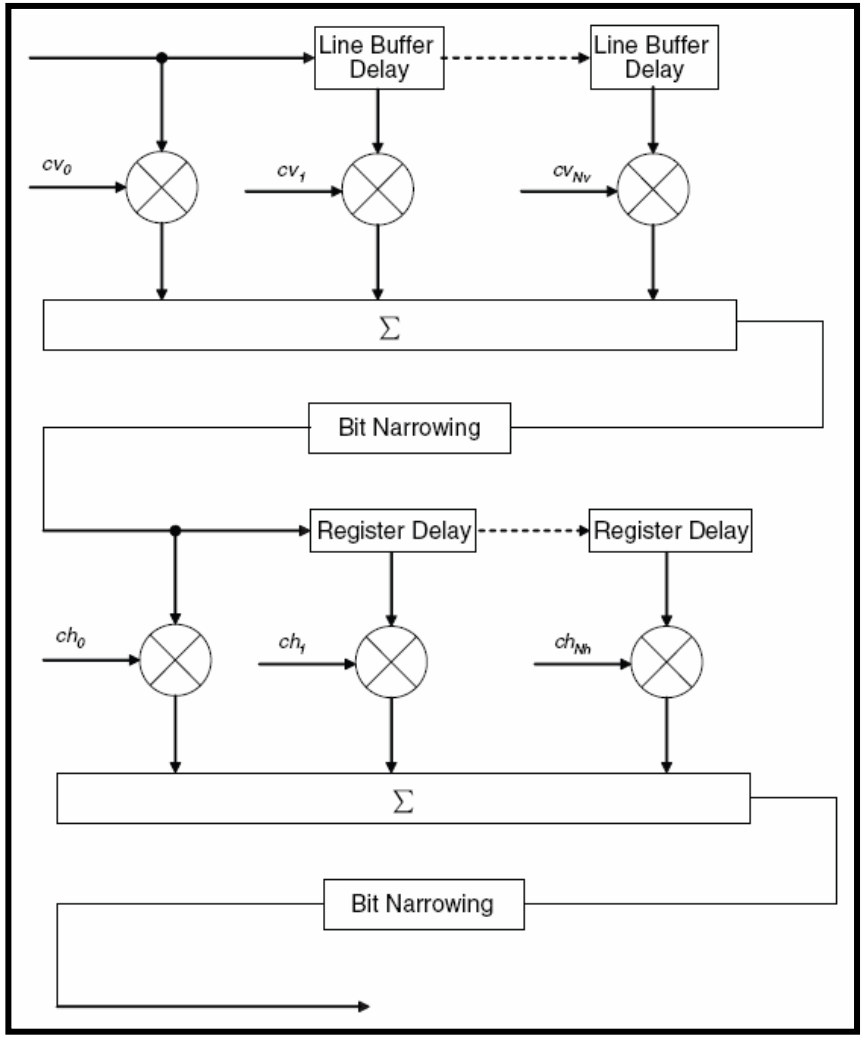
Scaler Vertical Coefficient Preview

Phase	Coeff 0	Coeff 1	Coeff 2	Coeff 3
0	0	128	0	0
1	-4	126	6	0
2	-8	124	13	-1
3	-10	119	20	-1
4	-11	111	30	-2
5	-11	103	40	-4
6	-10	93	50	-5
7	-9	82	61	-6
8	-8	72	72	-8
9	-6	61	82	-9
10	-5	50	93	-10
11	-4	40	103	-11
12	-2	30	111	-11
13	-1	20	119	-10
14	-1	13	124	-8
15	0	6	126	-4

Close

Polyphase Scaling Algorithm

- Data from multiple lines of the input image are assembled into line buffers – one for each vertical tap
- These data are then fed into parallel multipliers, before summation and possible loss of precision
- The results are gathered into registers – one for each horizontal tap
- These are again multiplied and summed before precision loss down to the output data bit width



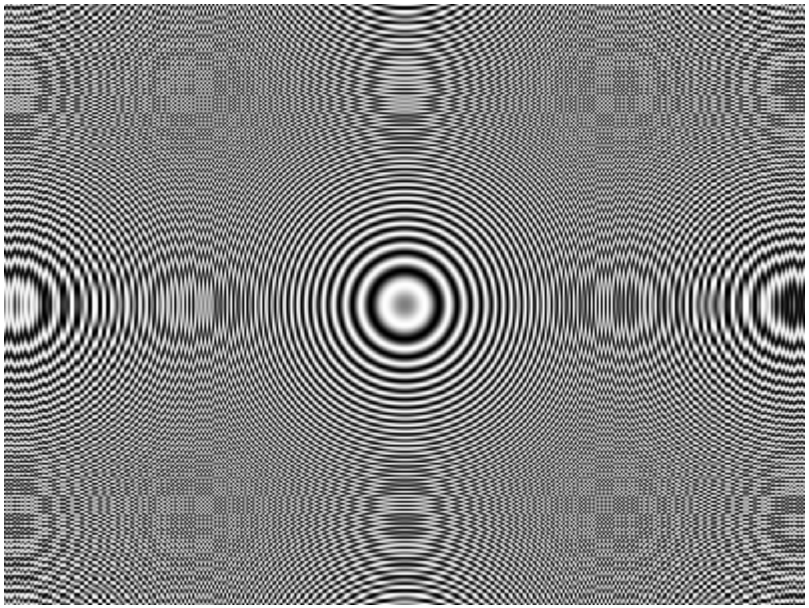
Polyphase Scaling Algorithm

- In polyphase mode, the parameters for the scaler function must be chosen carefully to get the best image quality
- Incorrect parameters can cause a decrease in image quality even as the resource usage increases
- The parameters which have the largest effect are the number of taps and the filter function chosen to provide the coefficients
- The number of phases and number of bits of precision used are less important to the image quality

Recommended parameters for the scaler function				
Scaling problem	**Taps**	**Phases**	**Precision**	**Coefficients**
Scaling up with any input/output resolution	**4**	**16**	**Signed, 1 integer bit, 7 fraction bits**	**Lanczos-2, or Bicubic**
Scaling down from *M* pixels to *N* pixels	$\frac{M \times 4}{N}$	**16**	**Signed, 1 integer bit, 7 fraction bits**	**Lanczos-2**
Scaling down from *M* pixels to *N* pixels (lower quality)	$\frac{M \times 2}{N}$	**16**	**Signed, 1 integer bit, 7 fraction bits**	**Lanczos-1**

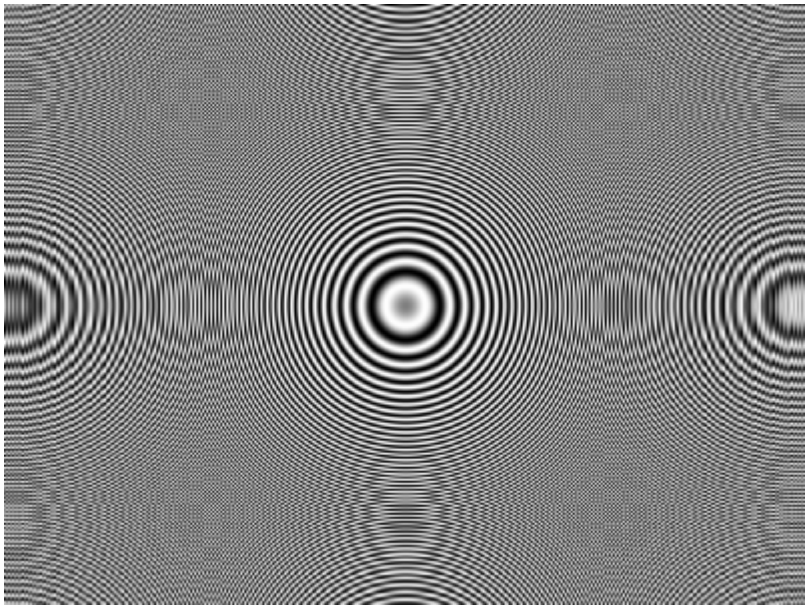

ORIGINAL IMAGE TO BE DOWNSCALED

Downscaling Using Nearest Neighbor Interpolation



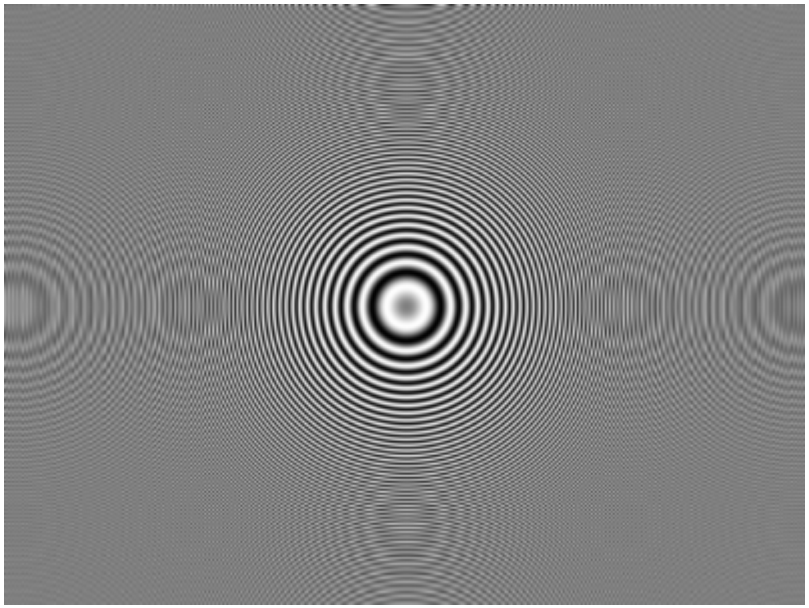
Nearest neighbor algorithm uses one neighboring pixel to interpolate.
This results in severe scaling artefacts.

Downscaling Using Bilinear Interpolation



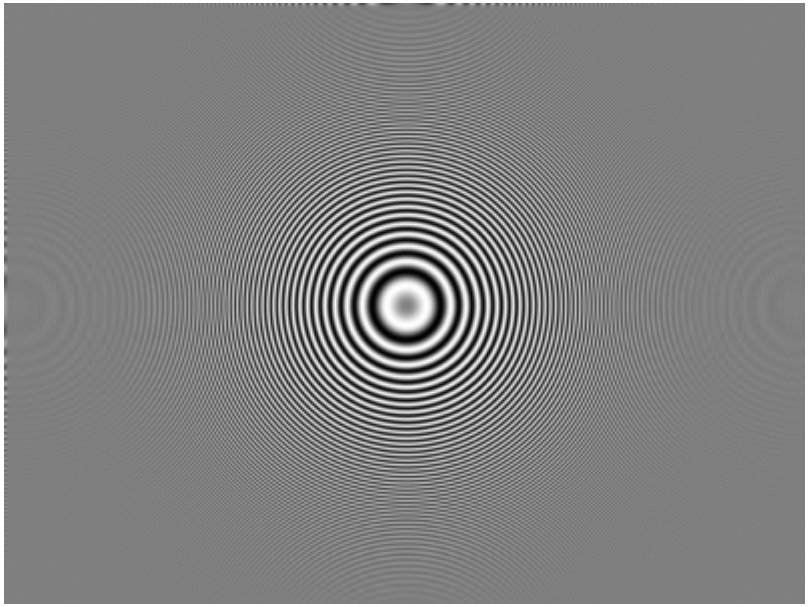
Bilinear algorithm uses a 2x2 matrix of pixels to interpolate.
This results in fewer (though significant) scaling artefacts.

Downscaling Using 5-Tap Lanczos-1 Interpolation



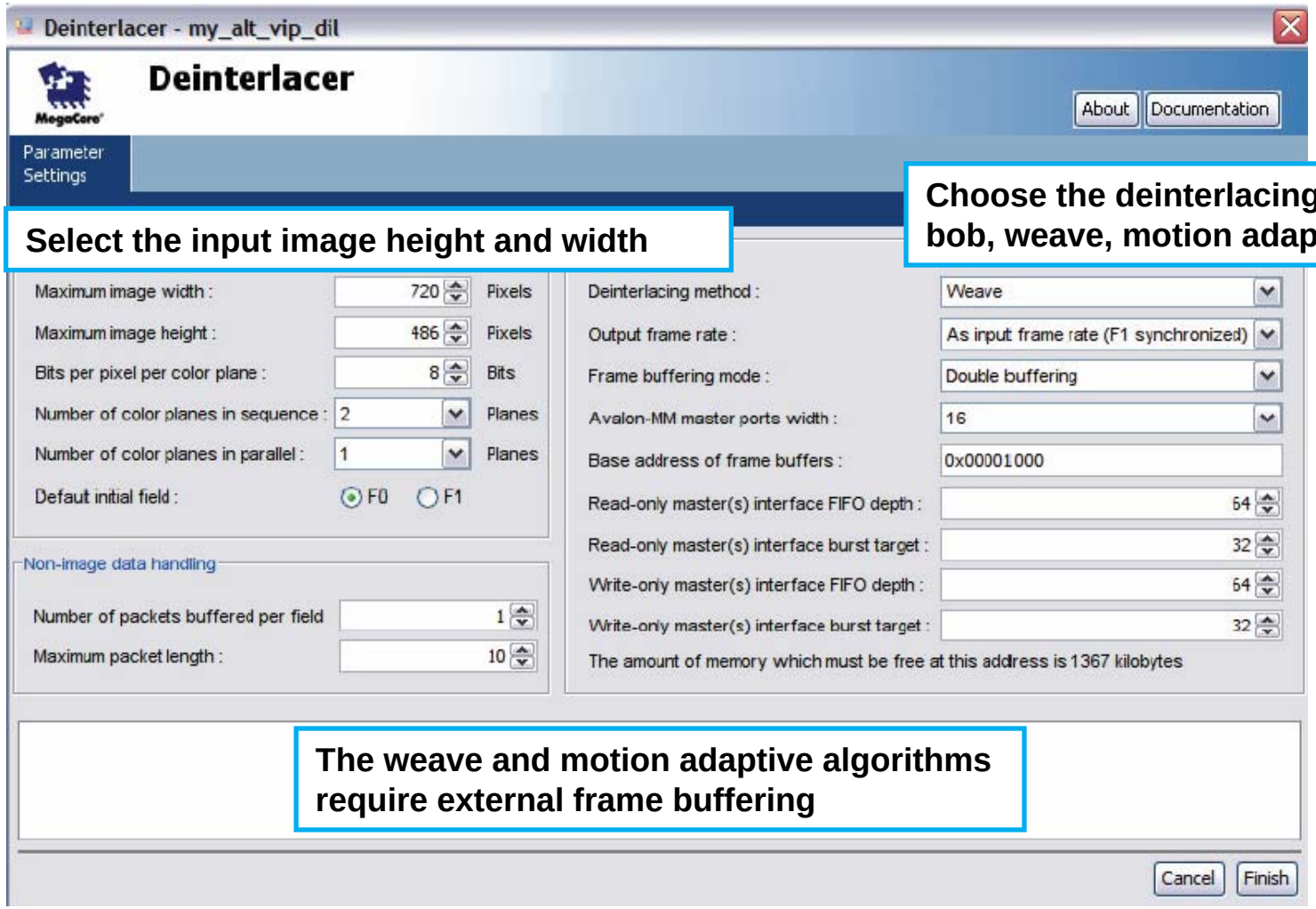
A 5-tap Lanczos-1 algorithm uses a 5x5 matrix of pixels to interpolate. This results in significantly reduced amount of scaling artefacts.

Downscaling Using 9-Tap Lanczos-2 Interpolation



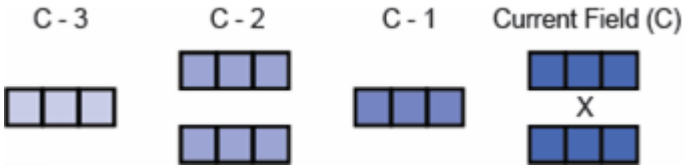
A 9-tap Lanczos-2 algorithm uses a 9x9 matrix of pixels to interpolate. This results in very high-quality scaling – at the expense of resources.

VIP Suite: Deinterlacer With Motion Adaptive Algorithm

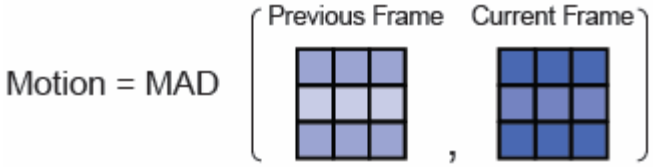


Motion Adaptive Deinterlacing

- Simple ***motion adaptive*** algorithm
- Pixels are collected from the current field and the three preceding it



- These pixels are assembled into two 3×3 groups of pixels and the minimum absolute difference (MAD) of the two groups is calculated



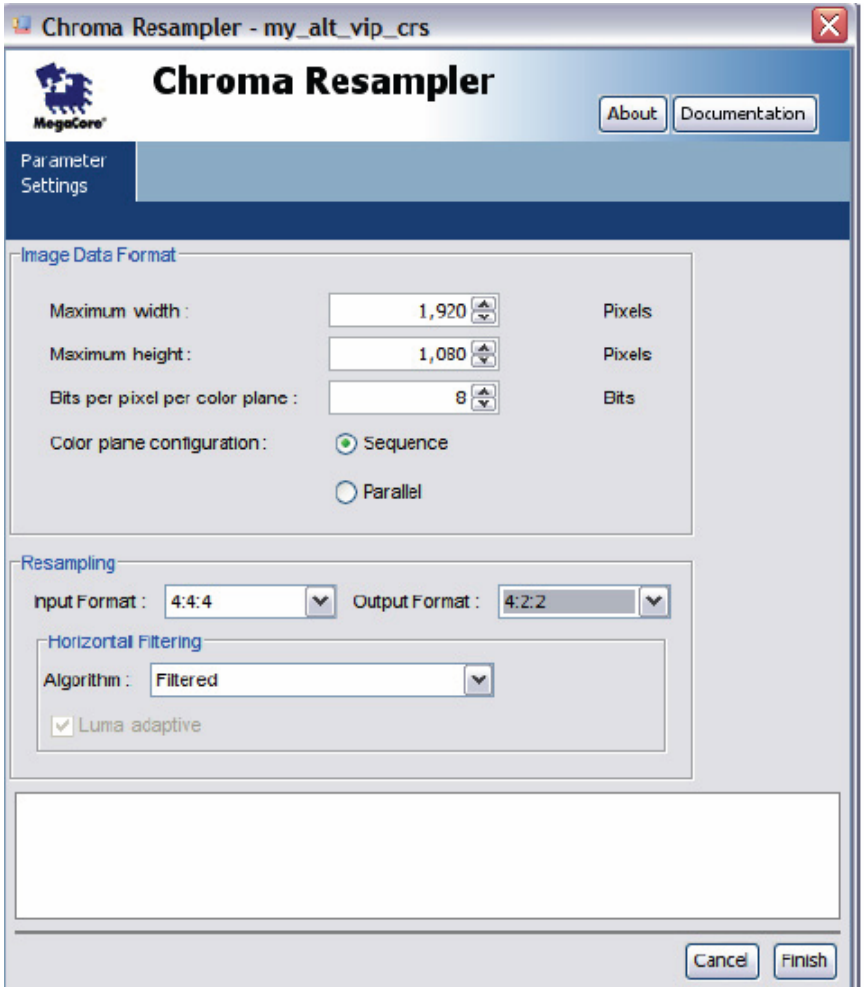
- Compare the MAD value with the previous MAD
  - Either the new value is kept or a mean of the new and old value is used

Chroma Downsampling Reduces the Bits/Frame

Image Size	Frame Size: (Total # of Pixels)	Frame Size: (Assume 10 bits per pixel and 4:4:4)	Frame Size: (Assume 10 bits per pixel and 4:2:2)	Frame Size: (Assume 10 bits per pixel and 4:2:0)
1920X1080p	1920 x 1080 = 2M pixels	60 Mbits	40 Mbits	30 Mbits
1920X1080i	1920 x 1080 x 0.5 = 1M pixels	30 Mbits	20 Mbits	15Mbits
1280X720p	1280 x 720 = 900K pixels	27 Mbits	18 Mbits	13.5 Mbits
SD 720x480i	720 x 480 x 0.5 = 173K pixels	5.19 Mbits	3.46 Mbits	2.595 Mbits

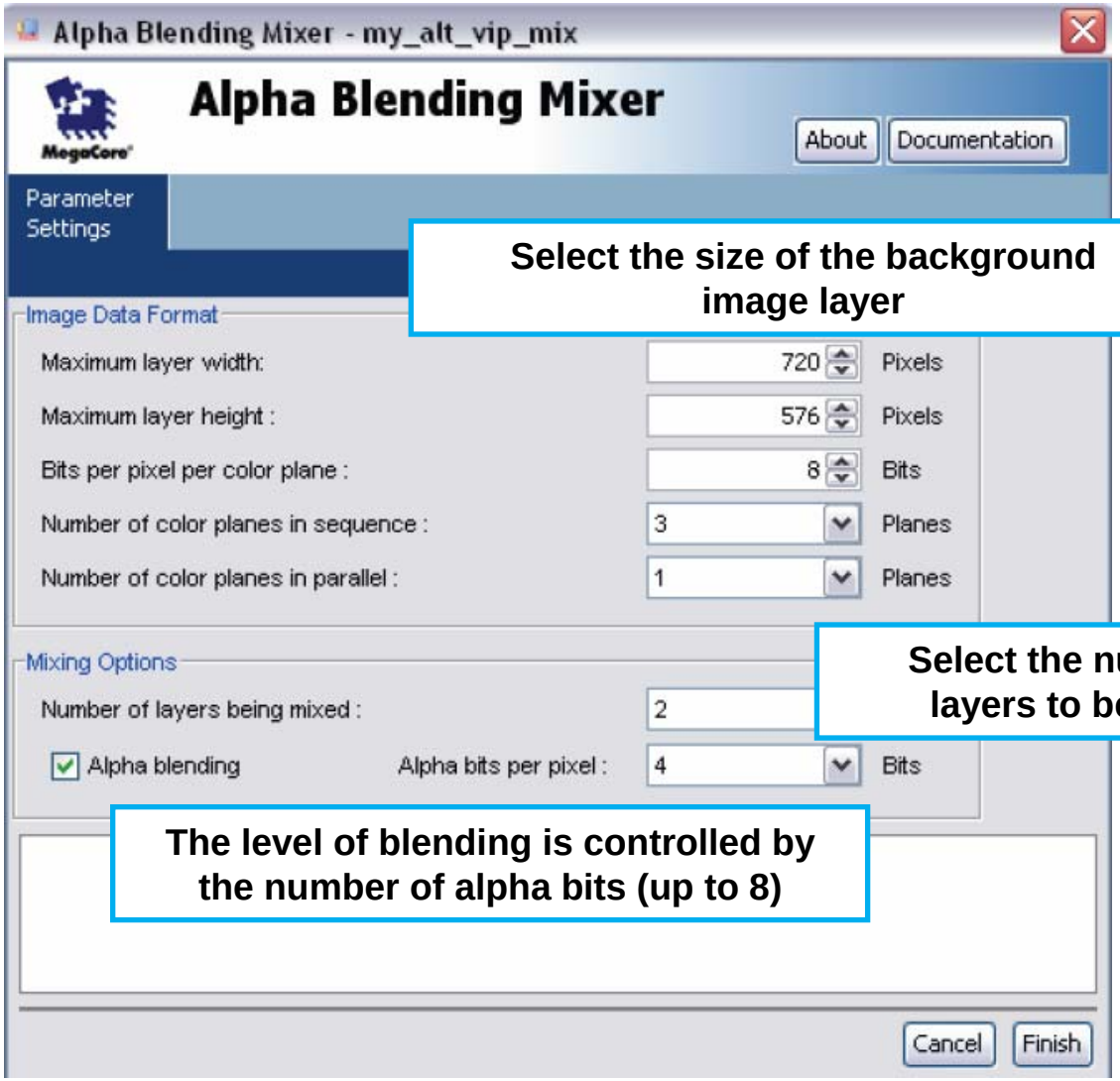
The numbers are not strictly accurate since HSYNC and VSYNC are not taken into account, but are meant to show the difference between a 4:4:4 and a 4:2:0 representation

VIP Suite: Multi-tap Filtered Chroma Resampler

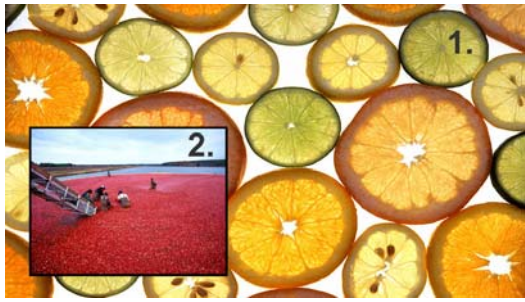


- The Chroma Resampler core allows you to change between 4:4:4, 4:2:2 and 4:2:0 sampling rates
- 4:4:4 → 4:2:2
  - The filtered algorithm for *down-sampling* uses a 9-tap filter with a fixed set of Lanczos-2 coefficients
- 4:2:2 → 4:4:4
  - The filtered algorithm for *up-sampling* uses a 4-tap filter with a fixed set of Lanczos-2 coefficients
- For both up-sampling and down-sampling, the vertical resampling (4:2:0) algorithm is fixed at nearest neighbor

VIP Suite: Alpha Blending Mixer



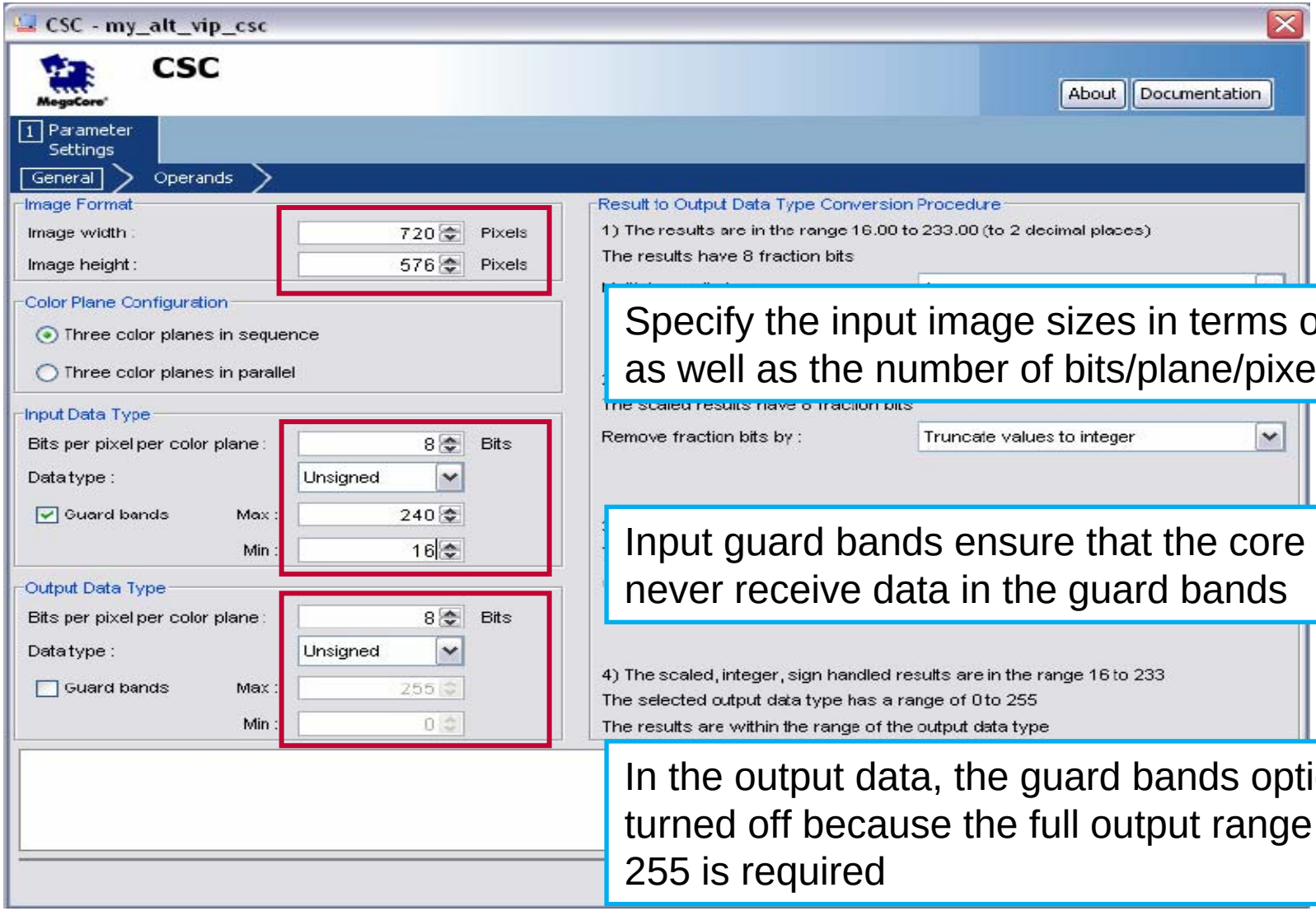
Select the size of the background image layer



Select the number of layers to be mixed

The level of blending is controlled by the number of alpha bits (up to 8)

VIP Suite: Color Space Conversion

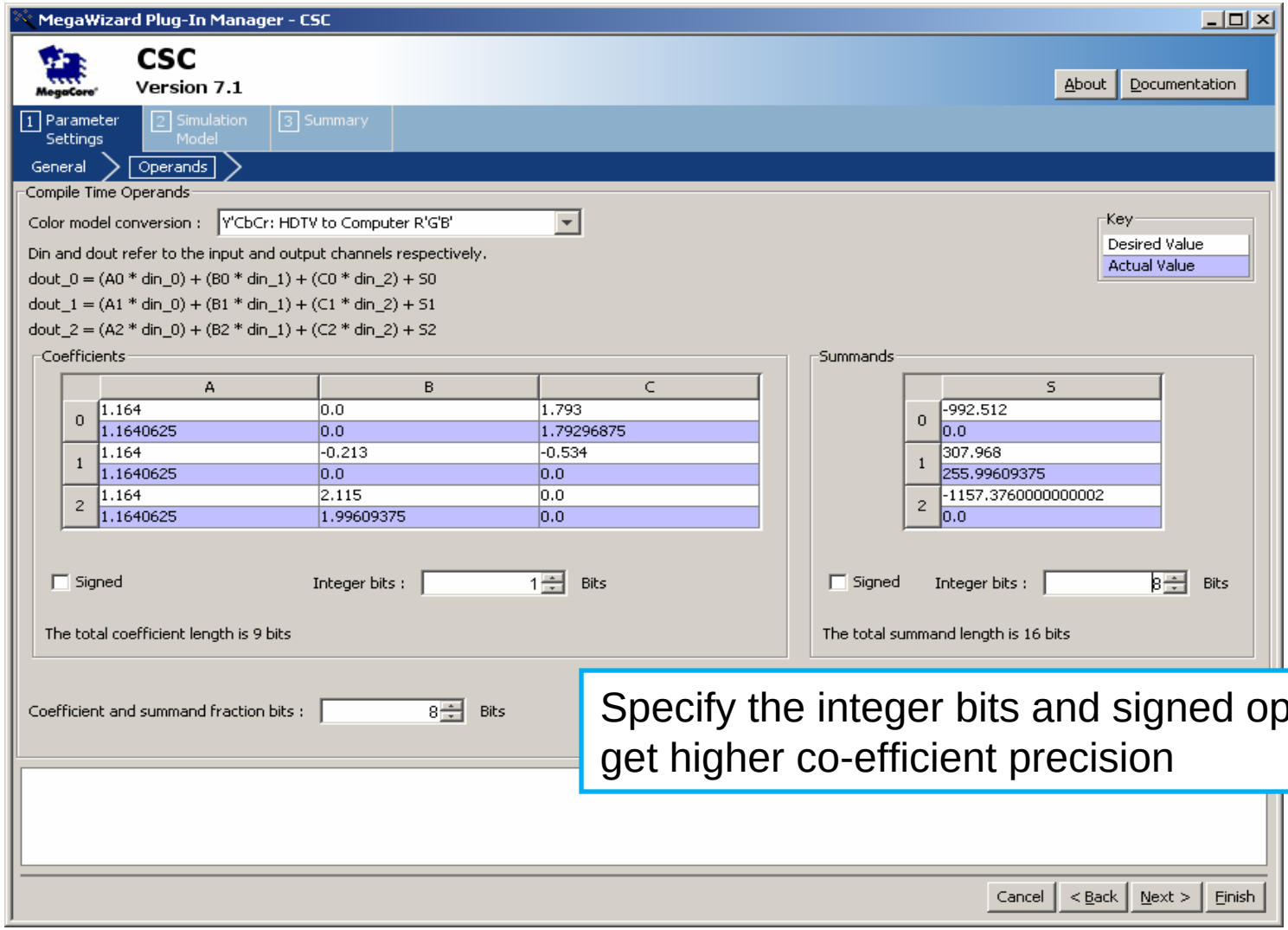


Specify the input image sizes in terms of pixels as well as the number of bits/plane/pixel

Input guard bands ensure that the core will never receive data in the guard bands

In the output data, the guard bands option is turned off because the full output range of 0 to 255 is required

VIP Suite: Color Space Conversion



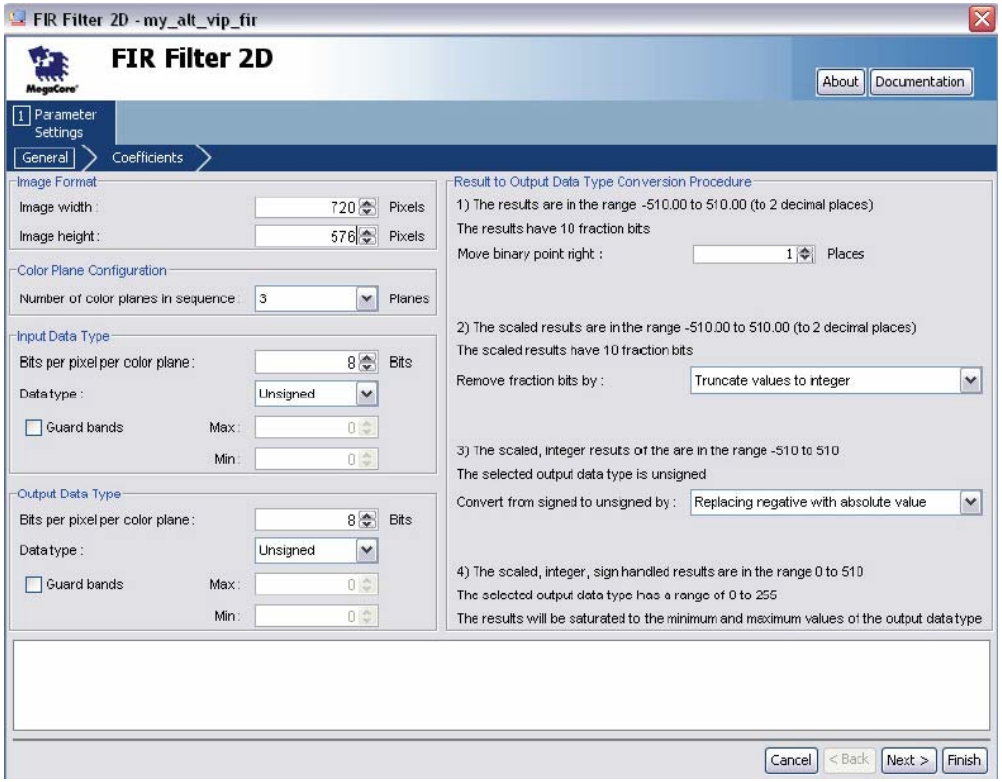
Specify the integer bits and signed option to get higher co-efficient precision

VIP Suite: 2D-FIR

- Various video/image processing signal chains have to filter the input signals to
  - Remove noise
  - Smoothen the image
  - Sharpen the image
  - Implement custom filtering
- The 2D-FIR filter function implements various custom filtering efficiently and quickly
- This core performs 2D convolution, using matrices of 3×3, 5×5, and 7×7 constant coefficients
- With suitable coefficients, the core can perform several operations including, but not limited to: sharpening, smoothing, and edge detection

VIP Suite: 2D-FIR

- An output pixel is calculated by
  - Multiplying input pixels in the kernel by the corresponding coefficient
  - Summing the values
- The output pixel value
  - Has its fractional bits removed
  - Is constrained to the output bit range
- The position of the output pixel corresponds to the mid point of the kernel



VIP Suite: 2D Median Filter

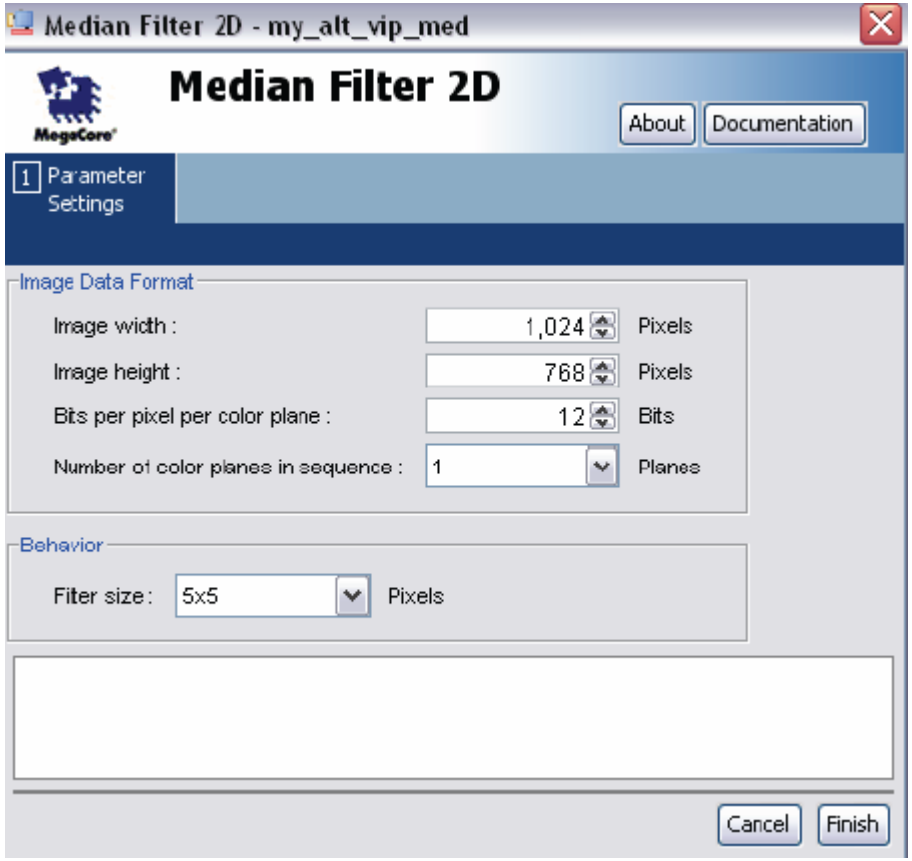
- Noise gets introduced into video data set via any electrical system used for storage, transmission, and/or processing

Median Filtering Is a Simple and Very Effective Noise Removal Filtering Process

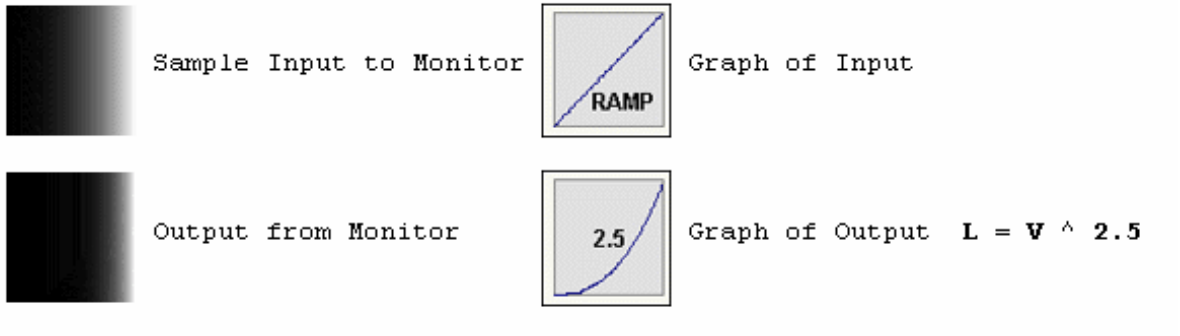
- Median filtering:
  - Each pixel is determined by the median value of all pixels in a selected neighborhood (mask, template, window)
  - The median value **m** of a population (set of pixels in a neighborhood) is that value in which half of the population has smaller values than **m**, and the other half has larger values than **m**

VIP Suite: 2D Median Filter

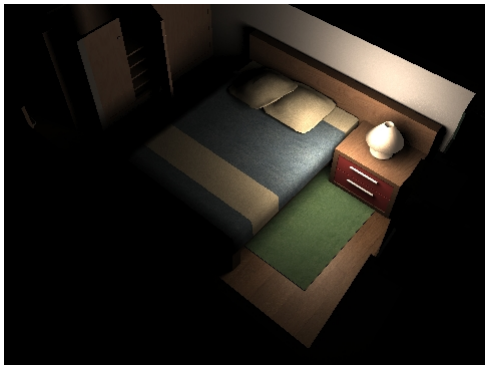
- The 2D median filter function provides a means to perform 2D median filtering operations using matrices of 3×3, 5×5, or 7×7 kernels
- Each output pixel is the median of the input pixels found in a 3x3, 5x5, or 7×7 kernel centered on the corresponding input pixel
- Larger kernel sizes require many more comparisons to perform the median filtering function; they also require correspondingly large increases in the number of logic elements used
- Larger sizes have a stronger effect, removing more noise but also potentially removing more detail

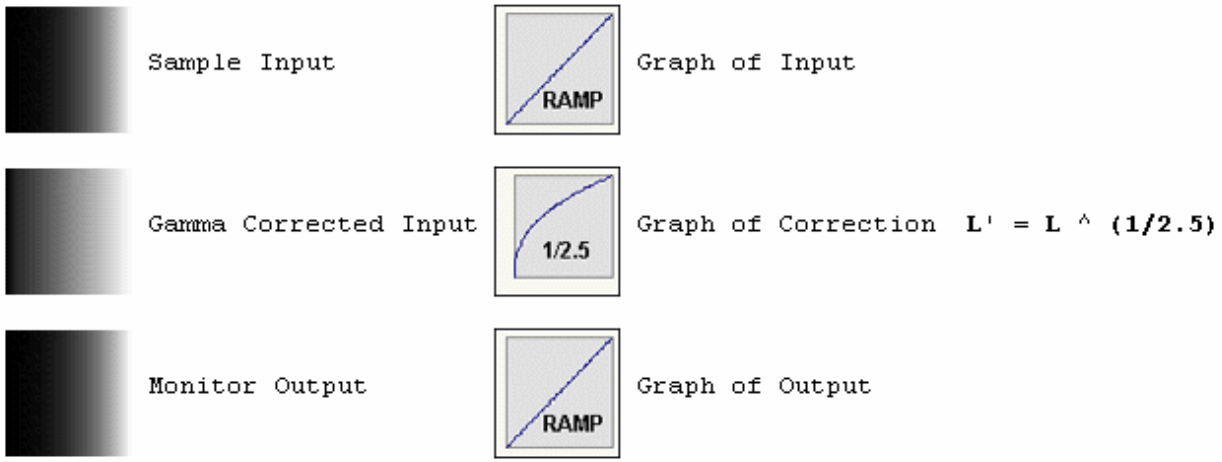


VIP Suite: Gamma Correction



NO Gamma Correction

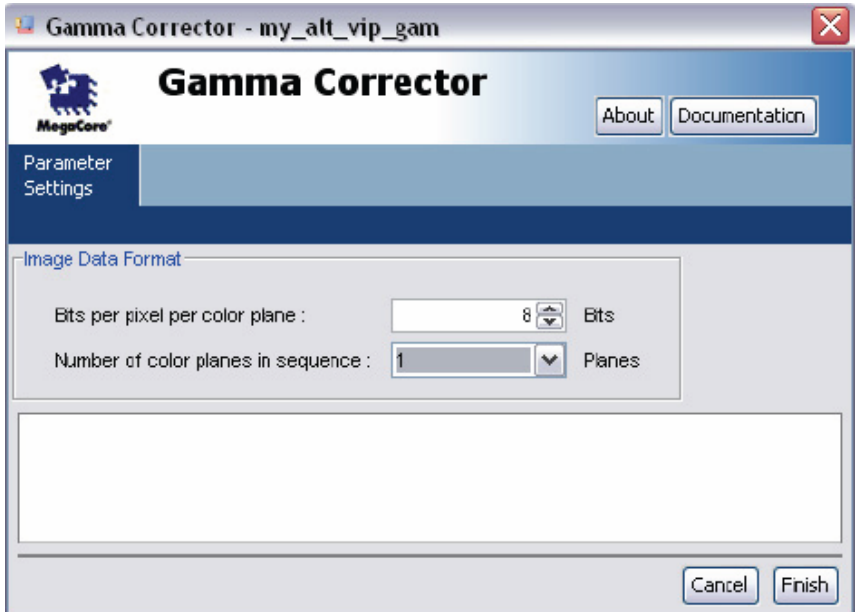




Gamma Correction 2.5

VIP Suite: Gamma Correction

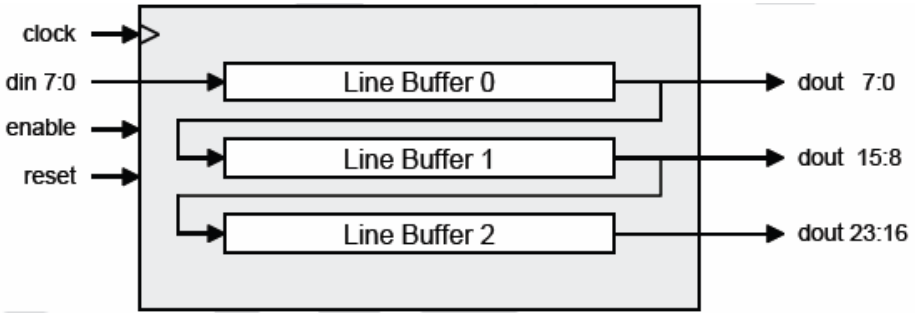
- The gamma corrector function provides a look-up table (LUT) accessed through an Avalon-MM slave port
- The gamma values can be entered into the LUT by external hardware using this interface



VIP Suite: Line Buffer Compiler

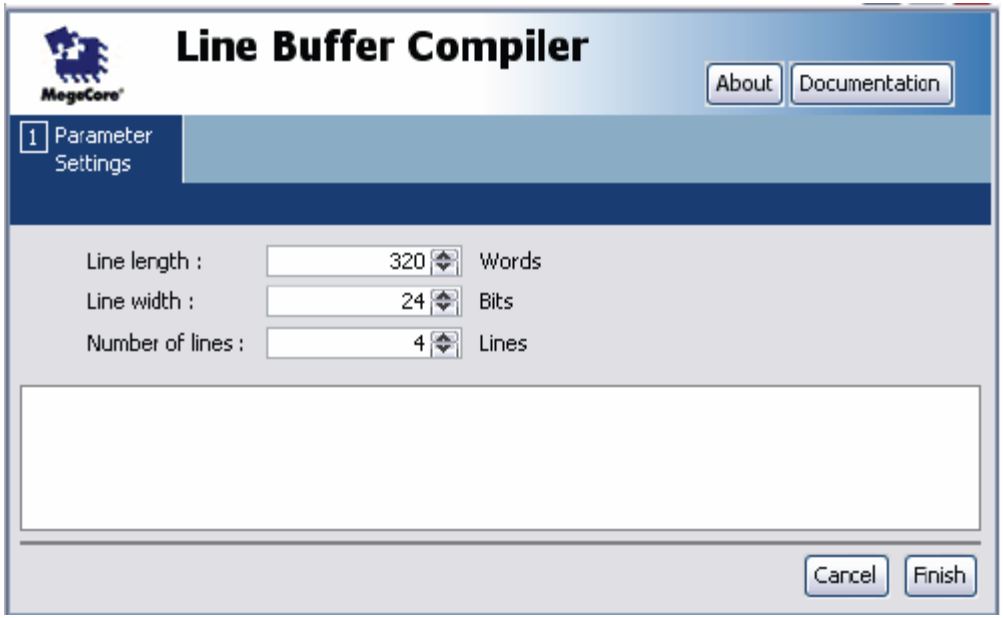
- FPGA memory is a valuable resource for many video and imaging applications
  - Particularly when developing HD systems and implementing high order accuracy algorithm

- The Line Buffer Compiler provides an efficient means to map line buffers on to Altera on-chip memories

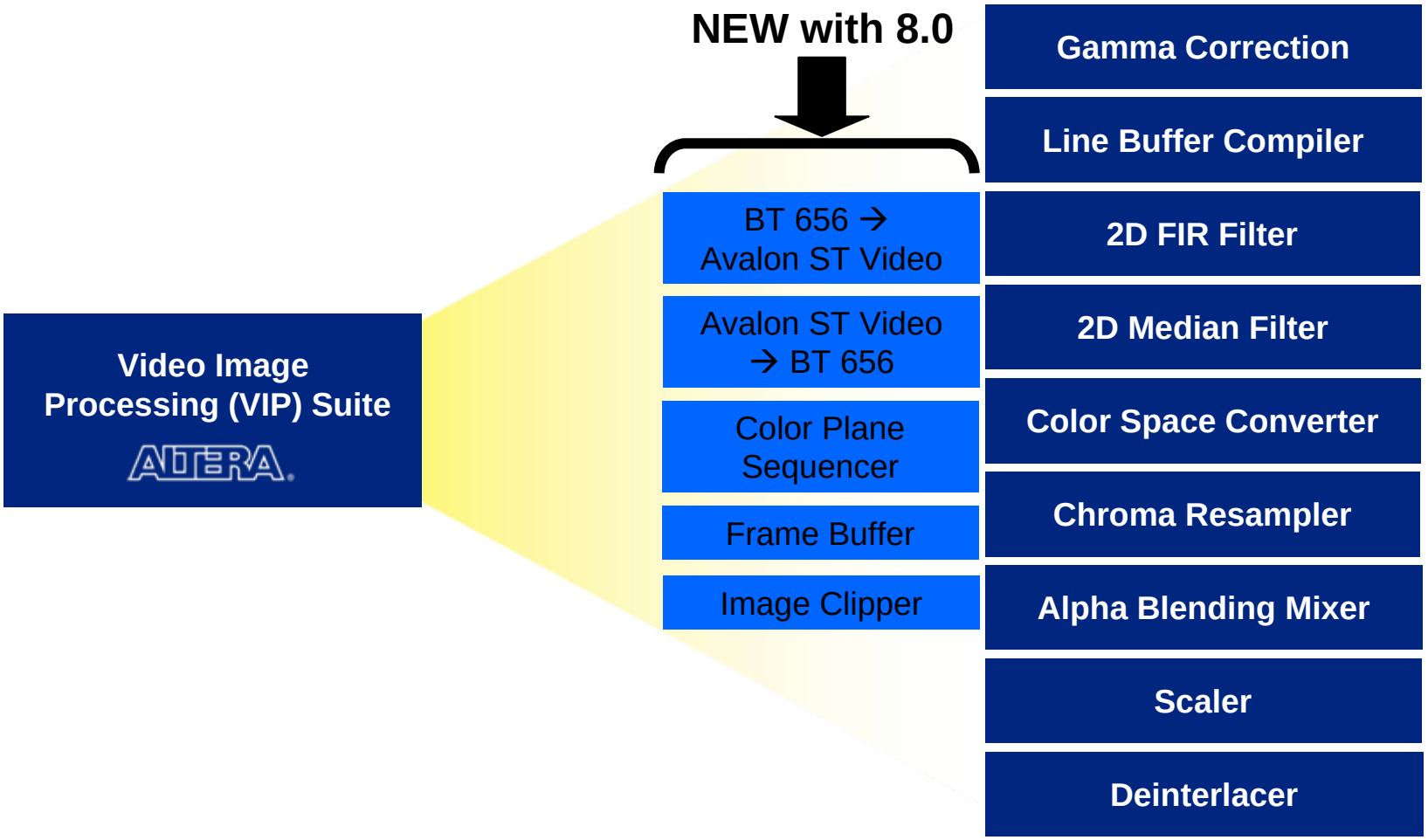


VIP Suite: Line Buffer Compiler

- To parameterize your Line Buffer Compiler function for a set of four line buffers each capable of holding 320 24-bit words…



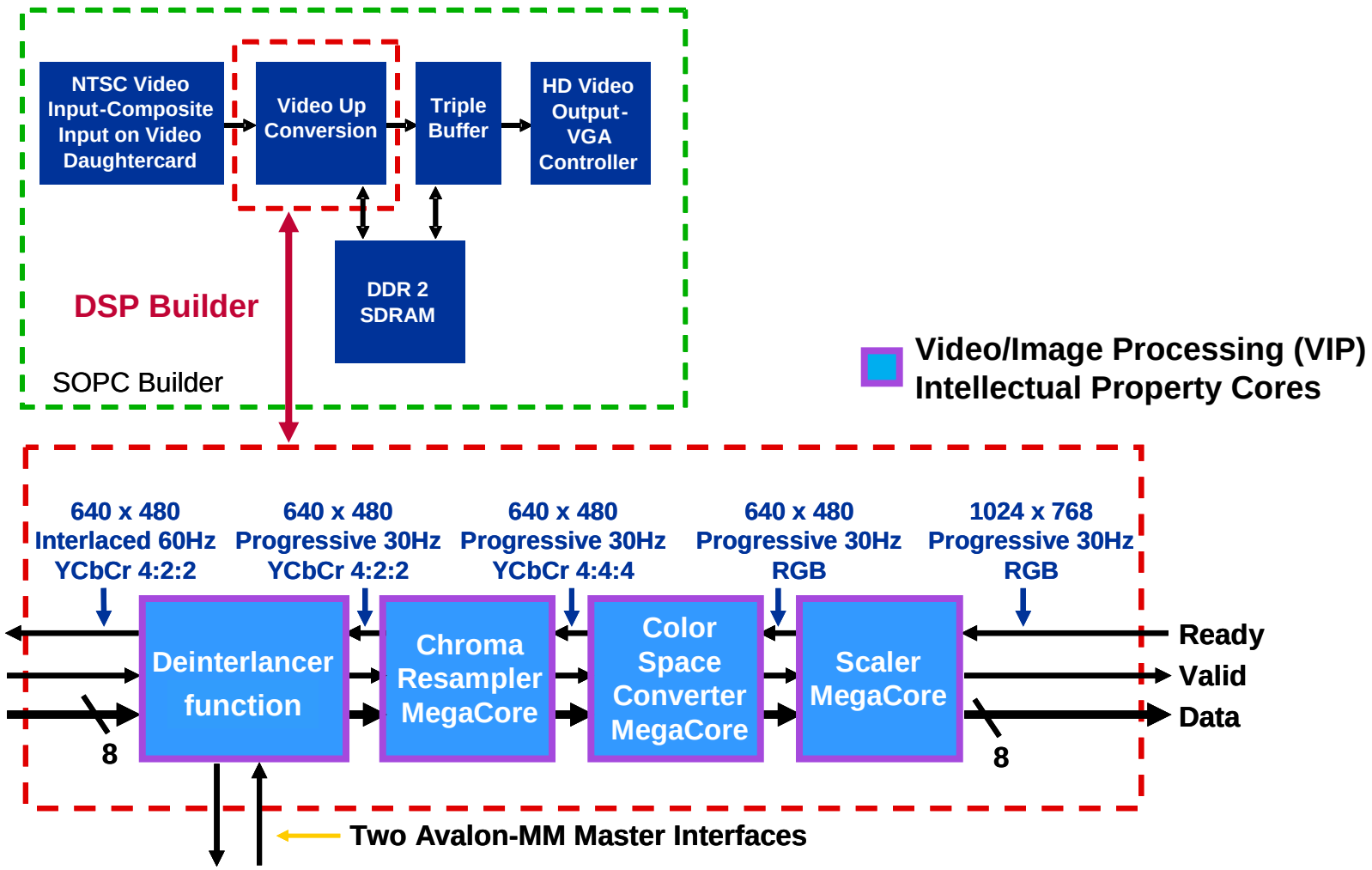
Video Image Processing (VIP)



Suite of building block IP for video processing

VIP Resources Available from Altera

Altera Video Reference Design



http://www.altera.com/end-markets/refdesigns/sys-sol/broadcast/ref-post-processing.html

Video Design Examples

DSP Design Examples

Table 1 contains digital signal processing (DSP) design examples for use in designs for Altera® devices. To see the design example, choose the corresponding icon in the Design Entry Method column.

Table 1. DSP Design Examples—Functions and Design Entry Methods

Function	Design Entry Method
Deinterlacer Using Weave Mode Updated	S
Deinterlacer Using Bob Mode Updated	S
Gamma Correction Updated	S
YCbCr to RGB Color Space Conversion Updated	S
Image Frame Resizing Using Scaler Updated	S
Salt and Pepper Noise Removal Using 2D Median Filter Updated	S
Video Picture in Picture (PIP) Mixing Using Alpha Blending Mixer Updated	S
Chroma Resampling Upconversion	S
2D Sharpening Finite Impulse Response (FIR) Filter Updated	S

http://www.altera.com/support/examples/dsp/exm-dsp.html

Cyclone III Video Kit

http://www.bitec.ltd.uk/ciii_video_dev_kit.html

- Altera EP3C120F780 development board
- Bitec HSMC Quad Video daughter card
  - 8 composite or 4 s-video inputs
  - 1 HD (1080p) DVI Output port or
  - 1 TV (PAL/NTSC) output with resolutions to 1024x768 and support for composite, s-video or SCART (RGB) outputs
- Bitec HSMC DVI daughter card
  - 1 HD (1080p) DVI Output port (HDMI with external adaptor)
  - 1 HD (1080p) DVI Input port (HDMI with external adaptor)
- Interfaces directly to the Altera Video and Image Processing (VIP) Suite

Stratix II GX Video Kit

http://www.altera.com/products/devkits/altera/kit-dsp-professional.html

- Stratix II GX video development board with a 2SGX90
- Video interfaces
  - Digital Video Interface (DVI) inputs/outputs
  - Four (4) standard definition (SD)/high definition (HD) SDI inputs/outputs, including Dual-Link SDI support
  - Asynchronous Serial Interface (ASI) inputs/outputs
- Audio interfaces
  - AES3
  - Sony/Phillips digital interface (S/PDIF)
- External memory
  - DDR2 DIMM (72 bit at 266 MHz)
  - 2-Mbyte SRAM
  - 16-Mbyte flash (configuration)

Summary

- Altera's video and image processing solution
  - Allows you to focus on your core competency
  - Eliminates the need to design, test, and debug standard video IP
  - Speeds up your development cycle

- Altera offers a complete programmable solution for your video application
  - IP (VIP Suite)
  - Development kits
  - Reference designs
  - Training