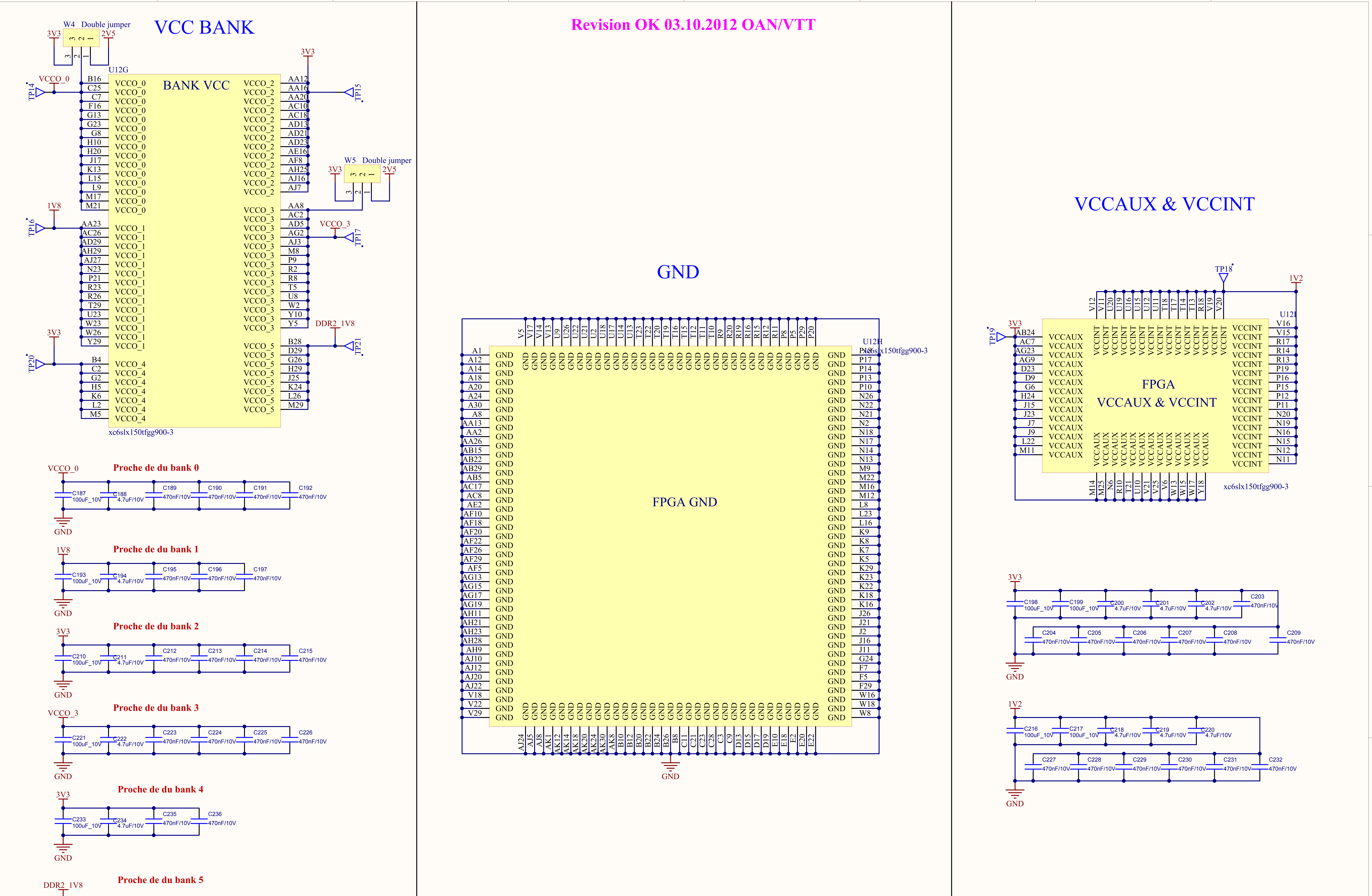
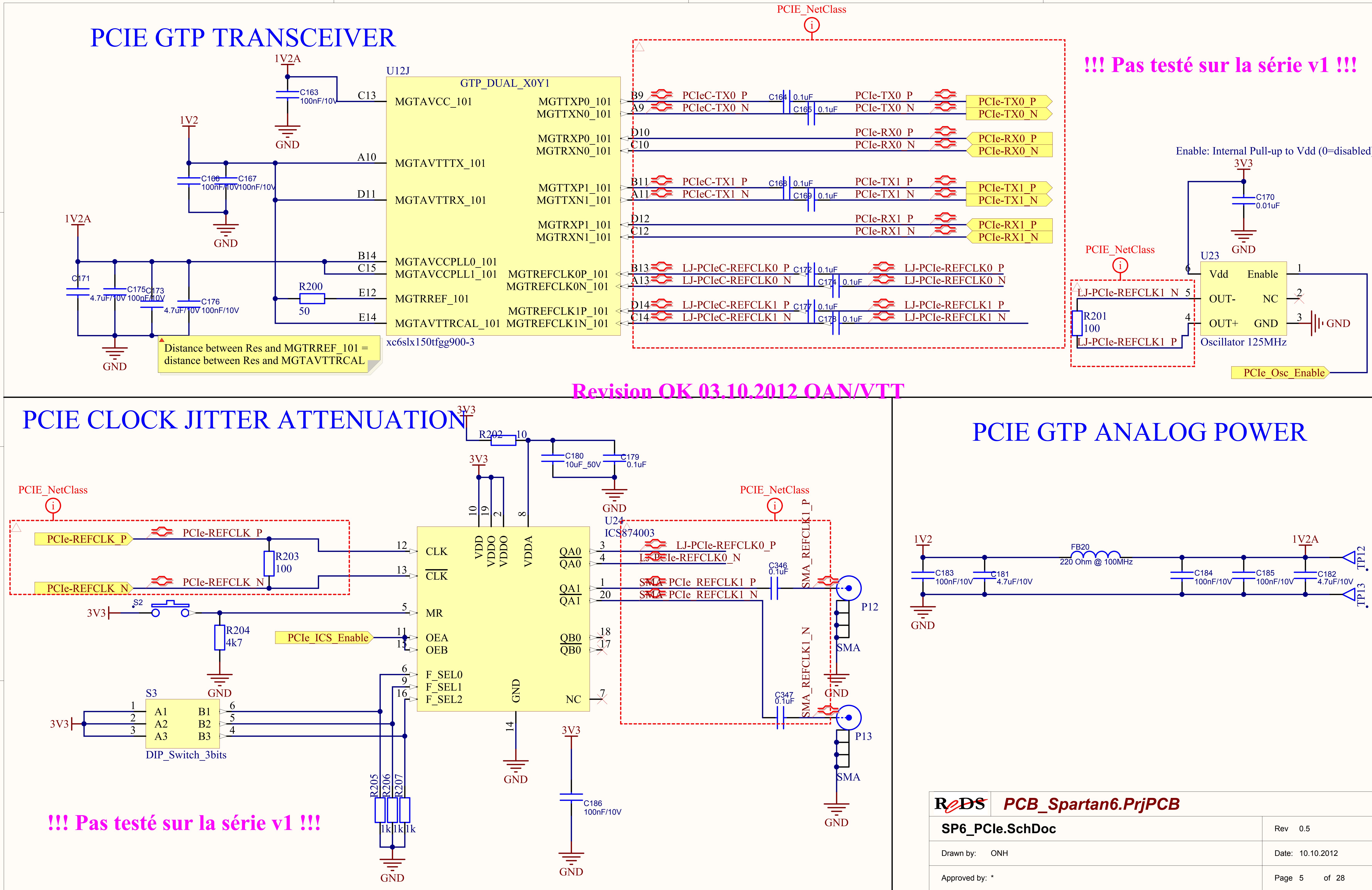

POWER 5V/16A
LTM4628
POWER 2.5V/8A
LTM4608A
POWER 1.25V/1.5A
LT1963A
POWER 1.8V/1.5A
LT1963A-1.8
POWER DDR2 1.8V/1.5A
POWER 3.3V/12A
LTM4601A
POWER 12V/5A
LTM4605
Revision OK 03.10.2012 OAN/VTT
PIN6 = TAB GND
LT1963A
LT1963A-1.5
LT1963A-1.8
$V_{OUT} = 1.21V\left(1+\frac{R2}{R1}\right)+(I_{ADJ})(R2)$
$V_{ADJ} = 1.21V$
$I_{ADJ} = 3\mu A$ AT 25°C
OUTPUT RANGE = 1.21V TO 20V
Analog 2.5V To place near U20
Analog 5.0V To place near U20
Power conn. 12A
VIN_7V_to_26V
PGOOD_5V
PGOOD_2V5
PGOOD_3V3
PGOOD_12V
PCB_Spartan6.PrjPCB
SP6_Board_Power.SchDoc
Rev 0.5
Drawn by: VTT
Date: 10.10.2012
Page 2 of 28



PCB_Spartan6.PrjPCB

SP6_Power.SchDoc

Drawn by: ONH	Rev 0.5
	Date: 10.10.2012
Approved by: *	Page 3 of 28



PCIE GTP TRANSCEIVER
!!! Pas testé sur la série v1 !!!
U12J
GTP_DUAL_X0Y1
MGTAVCC_101
MGTAVTTTX_101
MGTAVTTRX_101
MGTAVCCPLL0_101
MGTAVCCPLL1_101
MGTRREF_101
MGTAVTTRCAL_101
MGTTXP0_101
MGTTXN0_101
MGTRXP0_101
MGTRXN0_101
MGTTXP1_101
MGTTXN1_101
MGTRXP1_101
MGTRXN1_101
MGTREFCLK0P_101
MGTREFCLK0N_101
MGTREFCLK1P_101
MGTREFCLK1N_101
xc6slx150tfgg900-3
Distance between Res and MGTRREF_101 = distance between Res and MGTAVTTRCAL
PCIE_NetClass
PCIeC-TX0_P
PCIeC-TX0_N
PCIe-TX0_P
PCIe-TX0_N
PCIe-RX0_P
PCIe-RX0_N
PCIeC-TX1_P
PCIeC-TX1_N
PCIe-TX1_P
PCIe-TX1_N
PCIe-RX1_P
PCIe-RX1_N
LJ-PCIeC-REFCLK0_P
LJ-PCIeC-REFCLK0_N
LJ-PCIe-REFCLK0_P
LJ-PCIe-REFCLK0_N
LJ-PCIeC-REFCLK1_P
LJ-PCIeC-REFCLK1_N
LJ-PCIe-REFCLK1_P
LJ-PCIe-REFCLK1_N
Enable: Internal Pull-up to Vdd (0=disabled)
U23
Vdd
Enable
OUT-
NC
OUT+
GND
Oscillator 125MHz
PCIe_Osc_Enable
Revision OK 03.10.2012 OAN/VTT
PCIE CLOCK JITTER ATTENUATION
U24
ICS874003
PCIe-REFCLK_P
PCIe-REFCLK_N
CLK
MR
OEA
OEB
F_SEL0
F_SEL1
F_SEL2
VDD
VDDO
VDDA
QA0
QA1
QB0
NC
SMA_REFCLK1_P
SMA_REFCLK1_N
SMA-PCIe_REFCLK1_P
SMA-PCIe_REFCLK1_N
PCIe_ICS_Enable
DIP_Switch_3bits
P12
P13
SMA
!!! Pas testé sur la série v1 !!!
PCIE GTP ANALOG POWER
FB20
220 Ohm @ 100MHz
TP12
TP13
PCB_Spartan6.PrjPCB
SP6_PCIe.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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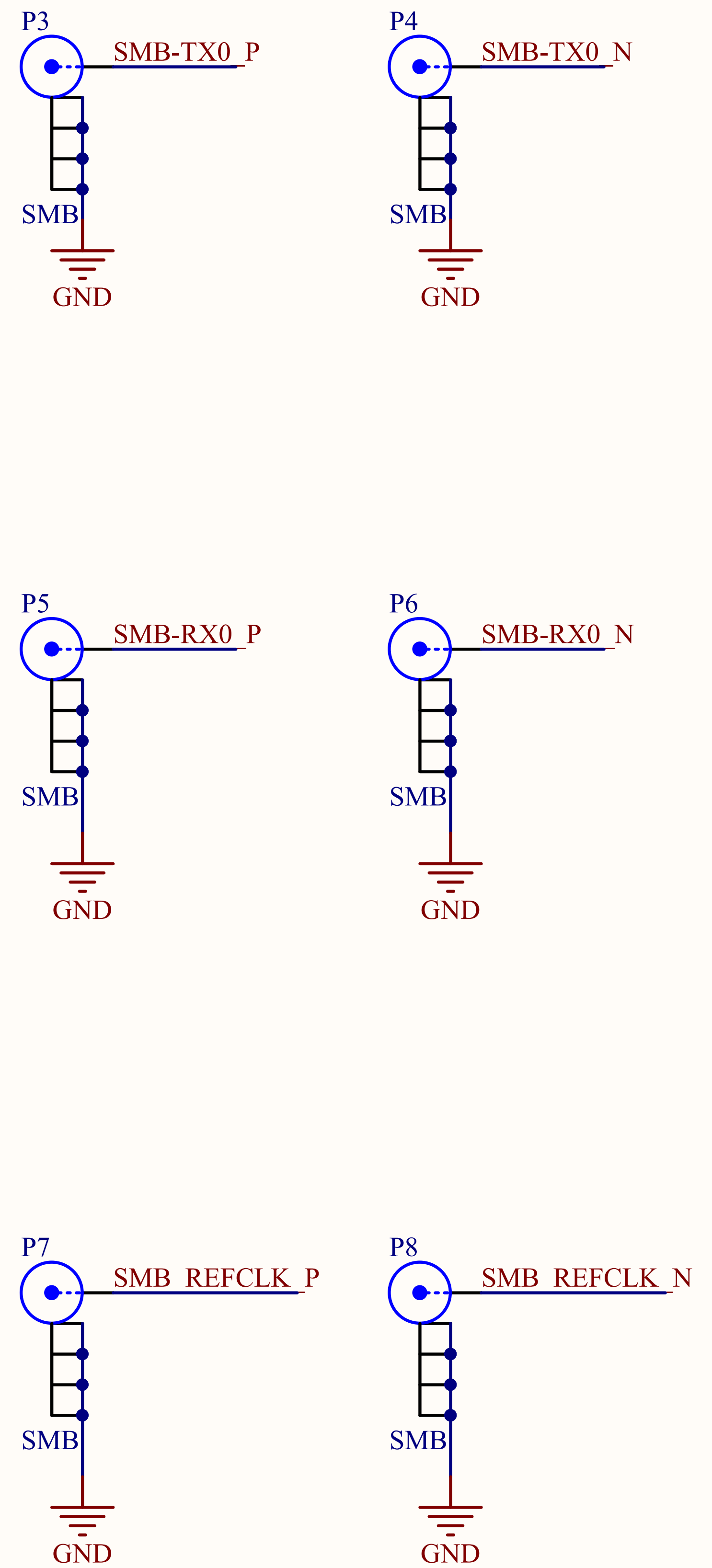
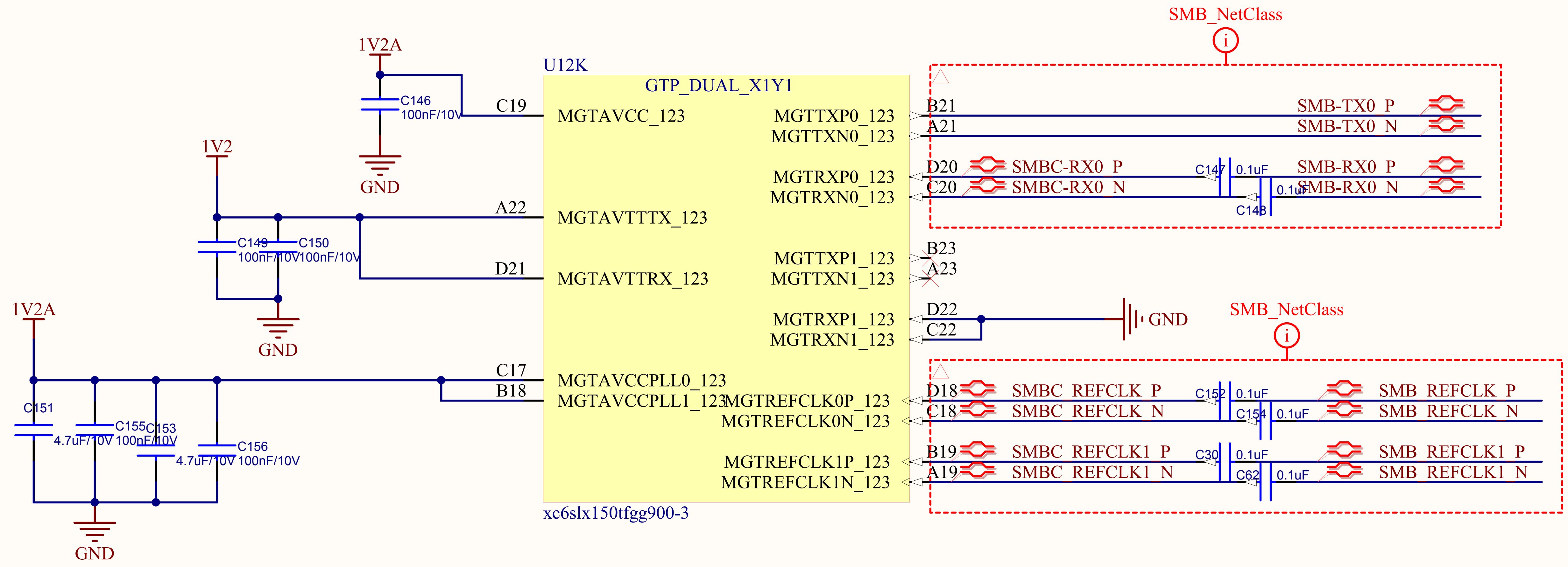
SMB CONNECTORS

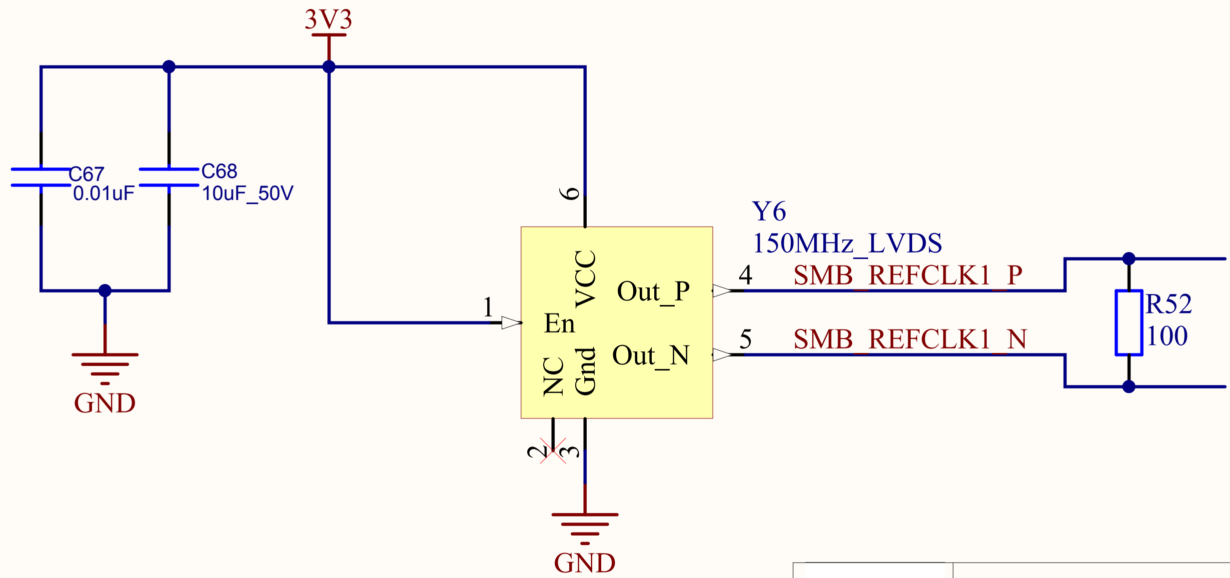


Revision OK 03.10.2012 OAN/VTT

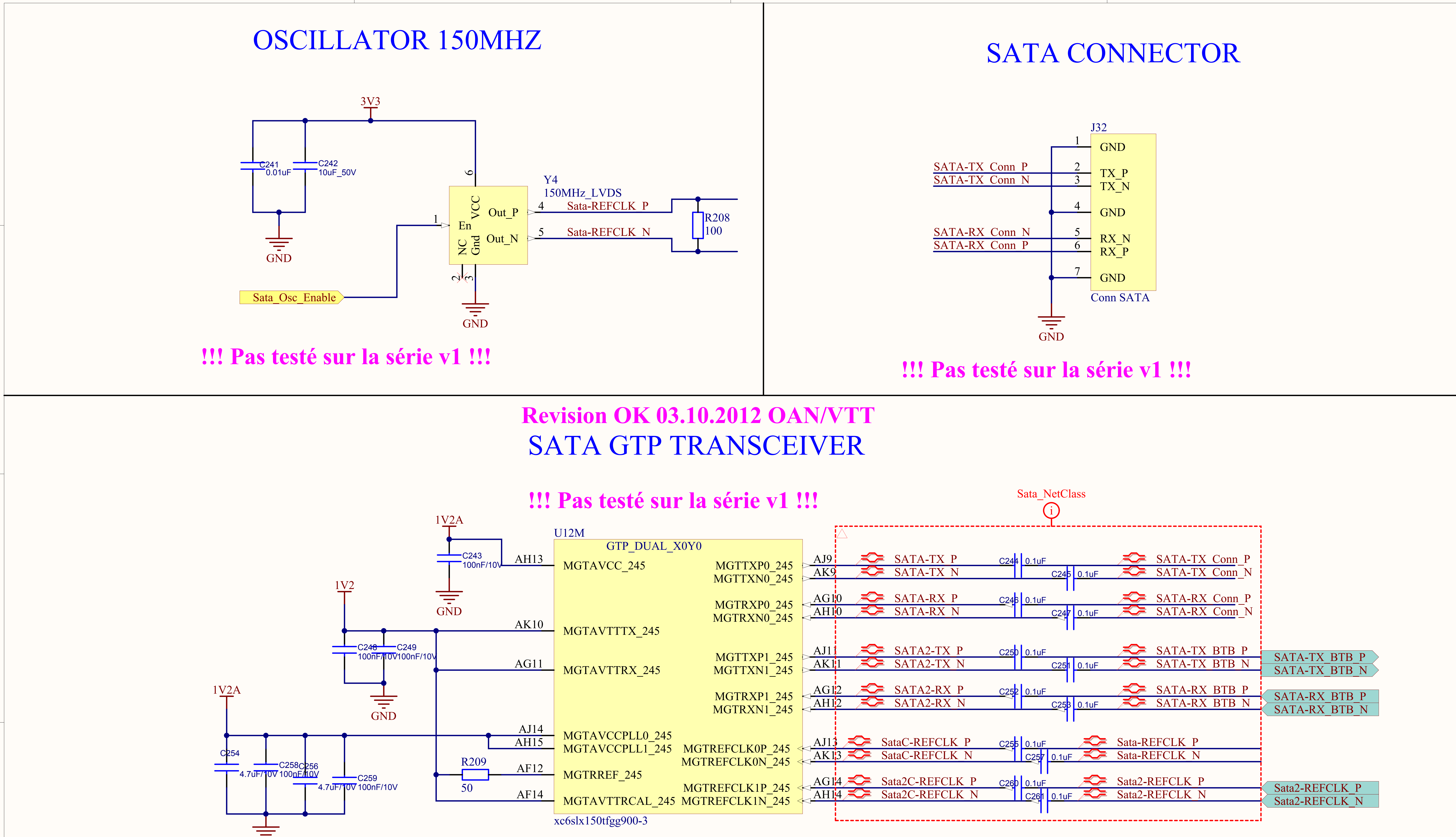
GTP TRANSCEIVER FOR SMB



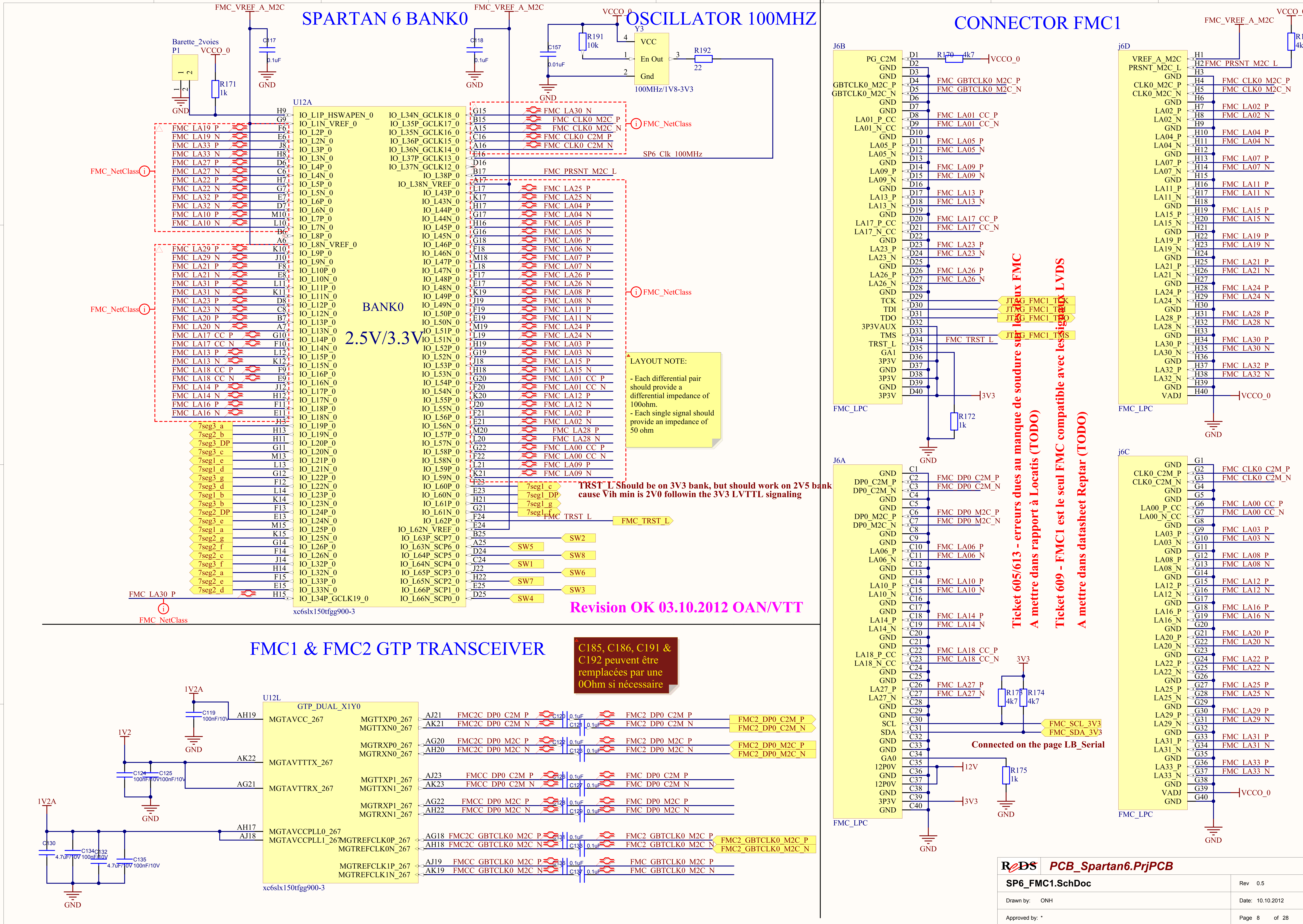
OSCILLATOR 150MHZ



ReDS	PCB_Spartan6.PrjPCB	
SP6_GTP_SMB.SchDoc		Rev 0.5
Drawn by: ONH		Date: 10.10.2012
Approved by: *		Page 6 of 28



PCB_Spartan6.PrjPCB		
SP6_SATA.SchDoc		Rev 0.5
Drawn by: ONH		Date: 10.10.2012
Approved by: *		Page 7 of 28


SPARTAN 6 BANK0
OSCILLATOR 100MHZ
CONNECTOR FMC1
FMC1 & FMC2 GTP TRANSCEIVER
BANK0
2.5V/3.3V
U12A
xc6slx150tfgg900-3
U12L
GTP_DUAL_X1Y0
100MHz/1V8-3V3
SP6_Clk_100MHz
FMC_NetClass
Barette_2voies
LAYOUT NOTE:
- Each differential pair should provide a differential impedance of 100ohm.
- Each single signal should provide an impedance of 50 ohm
TRST_L Should be on 3V3 bank, but should work on 2V5 bank cause Vih min is 2V0 followin the 3V3 LVTTL signaling
Revision OK 03.10.2012 OAN/VTT
C185, C186, C191 & C192 peuvent être remplacées par une 0Ohm si nécessaire
Ticket 605/613 - erreurs dues au manque de soudure sur les deux FMC
A mettre dans rapport à Locatis (TODO)
Ticket 609 - FMC1 est le seul FMC compatible avec les signaux LVDS
A mettre dans datasheet Reptar (TODO)
Connected on the page LB_Serial
J6B
J6A
j6D
j6C
FMC_LPC
JTAG_FMC1_TCK
JTAG_FMC1_TDI
JTAG_FMC1_TDO
JTAG_FMC1_TMS
FMC_TRST_L
FMC_PRSNT_M2C_L
FMC_SCL_3V3
FMC_SDA_3V3
PCB_Spartan6.PrjPCB
SP6_FMC1.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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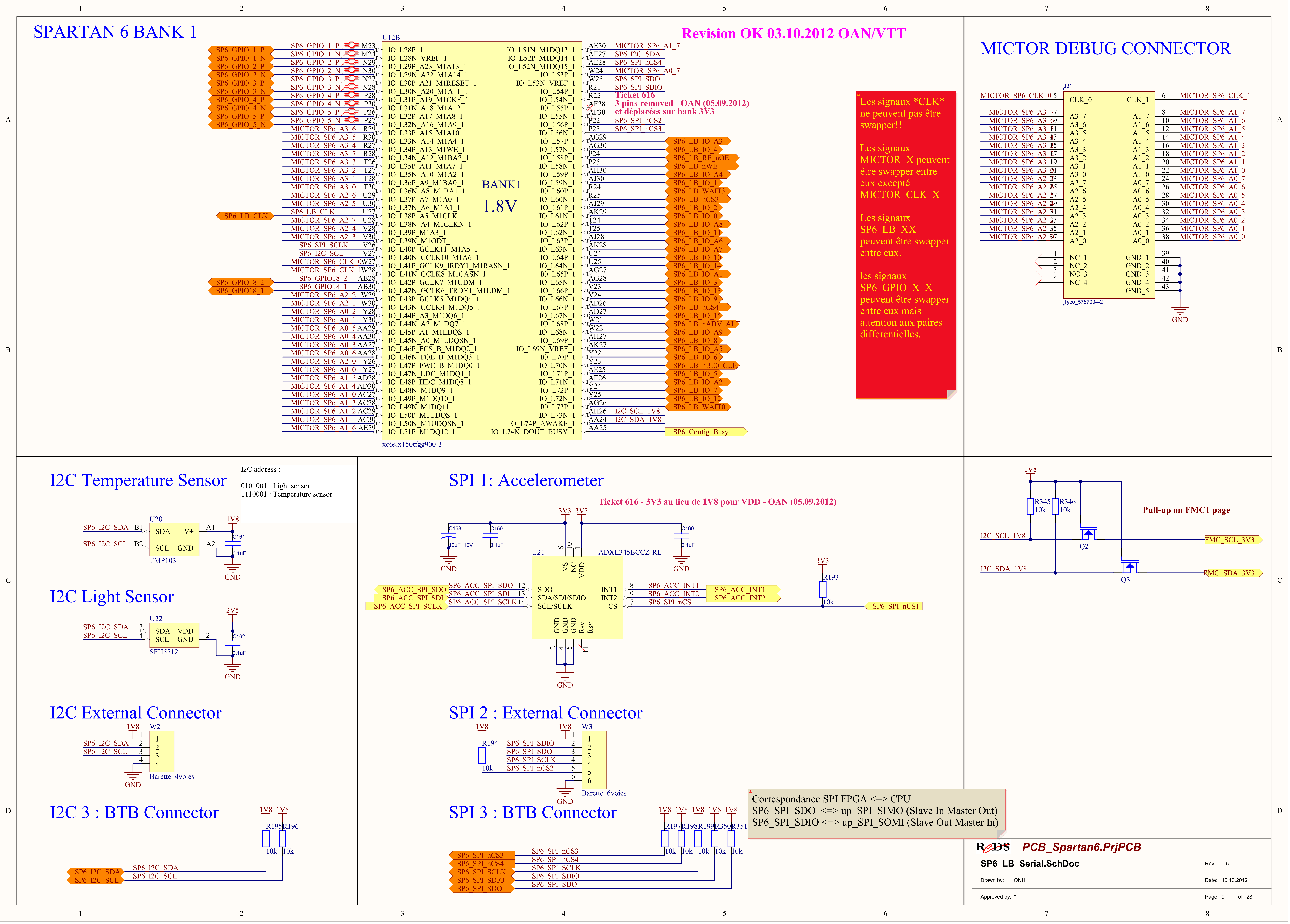

SPARTAN 6 BANK 1
Revision OK 03.10.2012 OAN/VTT
U12B
BANK1
1.8V
xc6slx150tfgg900-3
Ticket 616
3 pins removed - OAN (05.09.2012)
et déplacées sur bank 3V3
MICTOR DEBUG CONNECTOR
J31
Tyco_5767004-2
Les signaux *CLK* ne peuvent pas être swapper!!
Les signaux MICTOR_X peuvent être swapper entre eux excepté MICTOR_CLK_X
Les signaux SP6_LB_XX peuvent être swapper entre eux.
les signaux SP6_GPIO_X_X peuvent être swapper entre eux mais attention aux paires differentielles.
I2C Temperature Sensor
I2C address :
0101001 : Light sensor
1110001 : Temperature sensor
U20
TMP103
I2C Light Sensor
U22
SFH5712
I2C External Connector
W2
Barette_4voies
I2C 3 : BTB Connector
SPI 1: Accelerometer
Ticket 616 - 3V3 au lieu de 1V8 pour VDD - OAN (05.09.2012)
U21
ADXL345BCCZ-RL
SPI 2 : External Connector
W3
Barette_6voies
SPI 3 : BTB Connector
Pull-up on FMC1 page
Correspondance SPI FPGA <=> CPU
SP6_SPI_SDO <=> up_SPI_SIMO (Slave In Master Out)
SP6_SPI_SDIO <=> up_SPI_SOMI (Slave Out Master In)
REDS
PCB_Spartan6.PrjPCB
SP6_LB_Serial.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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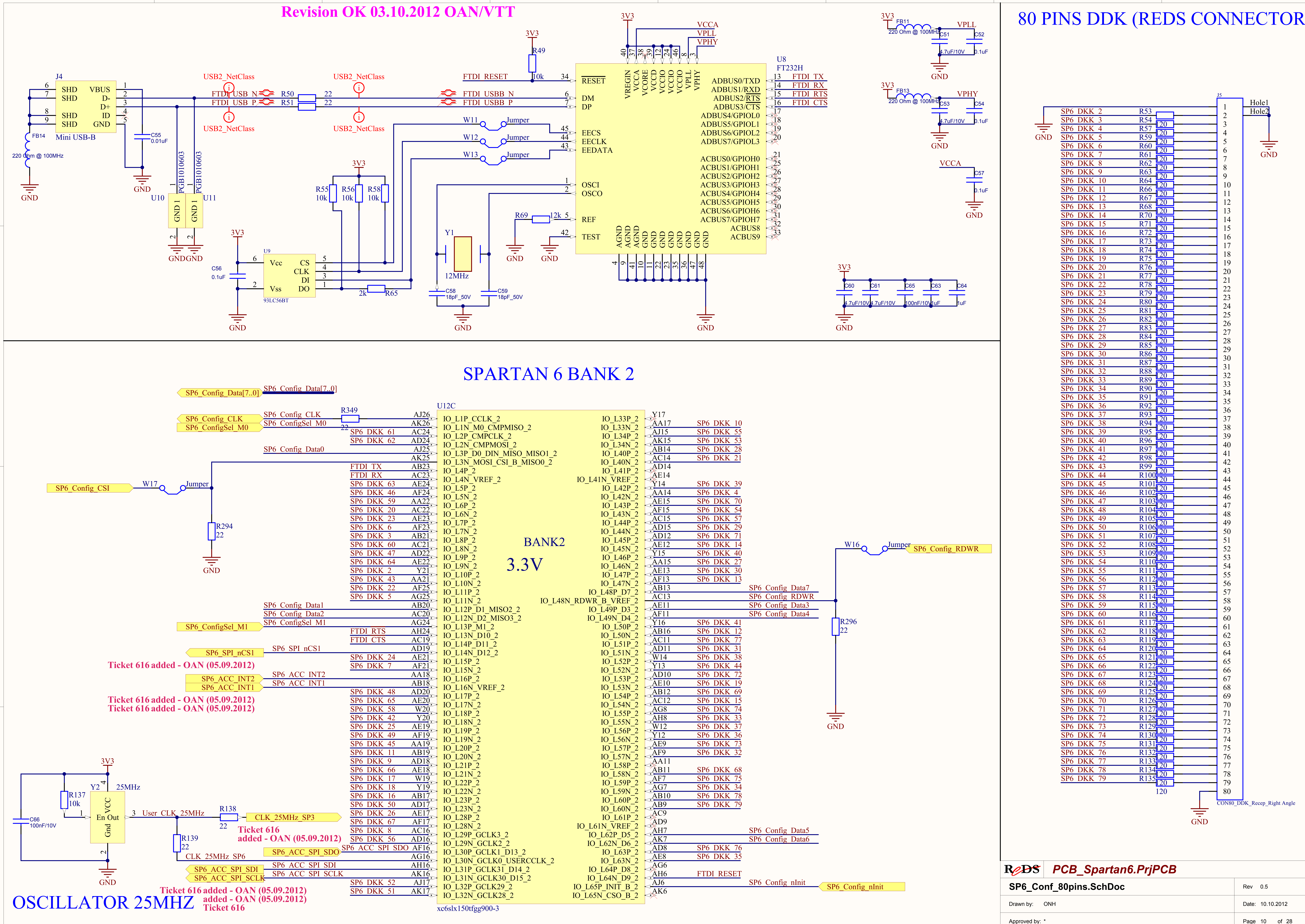
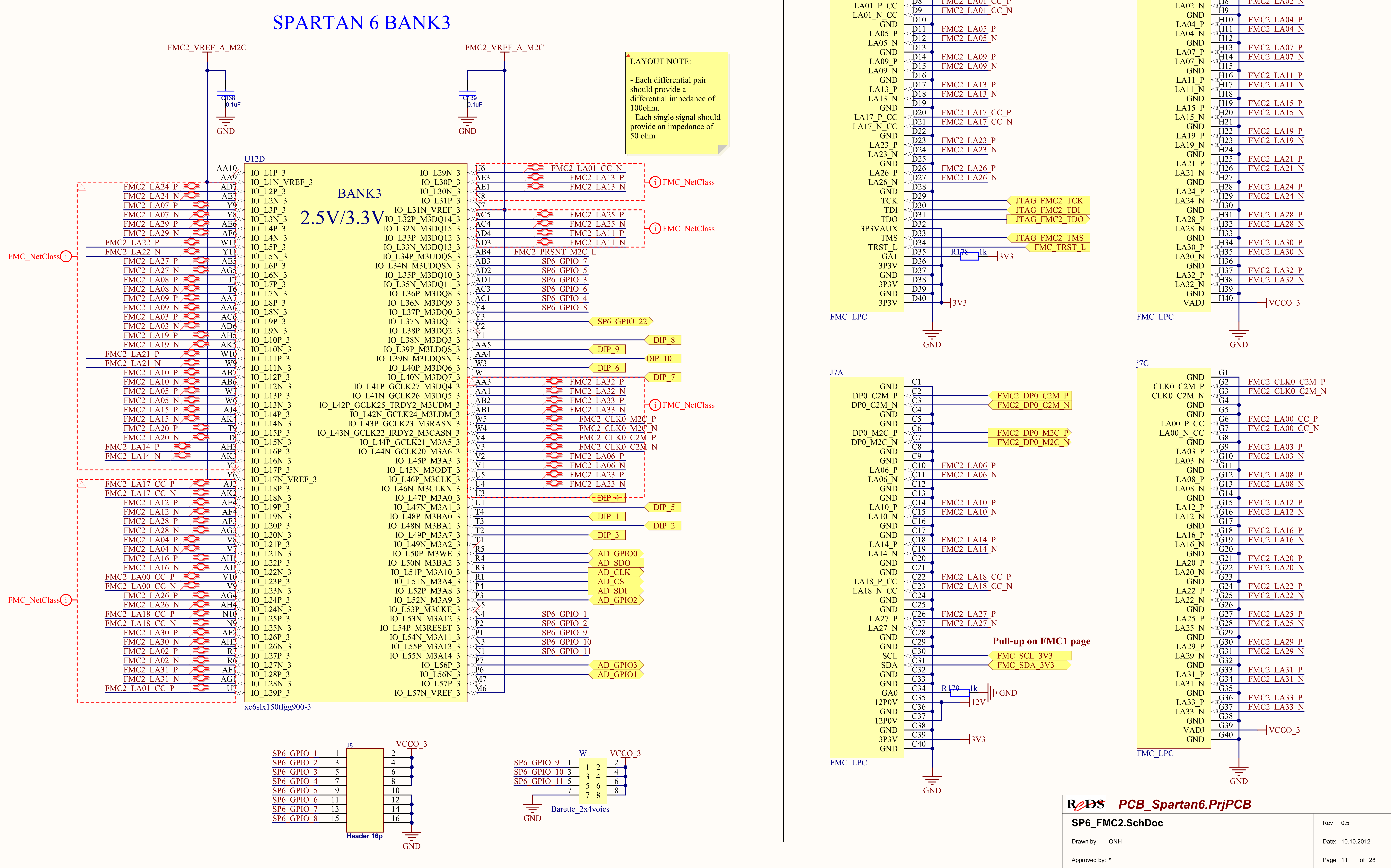

Revision OK 03.10.2012 OAN/VTT
80 PINS DDK (REDS CONNECTOR)
SPARTAN 6 BANK 2
BANK2
3.3V
OSCILLATOR 25MHZ
FT232H
Mini USB-B
93LC56BT
12MHz
CON80_DDK_Recep_Right Angle
xc6slx150tfgg900-3
Ticket 616 added - OAN (05.09.2012)
Ticket 616 added - OAN (05.09.2012)
Ticket 616 added - OAN (05.09.2012)
Ticket 616 added - OAN (05.09.2012)
Ticket 616 added - OAN (05.09.2012)
Ticket 616 added - OAN (05.09.2012)
PCB_Spartan6.PrjPCB
SP6_Conf_80pins.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
Page 10 of 28

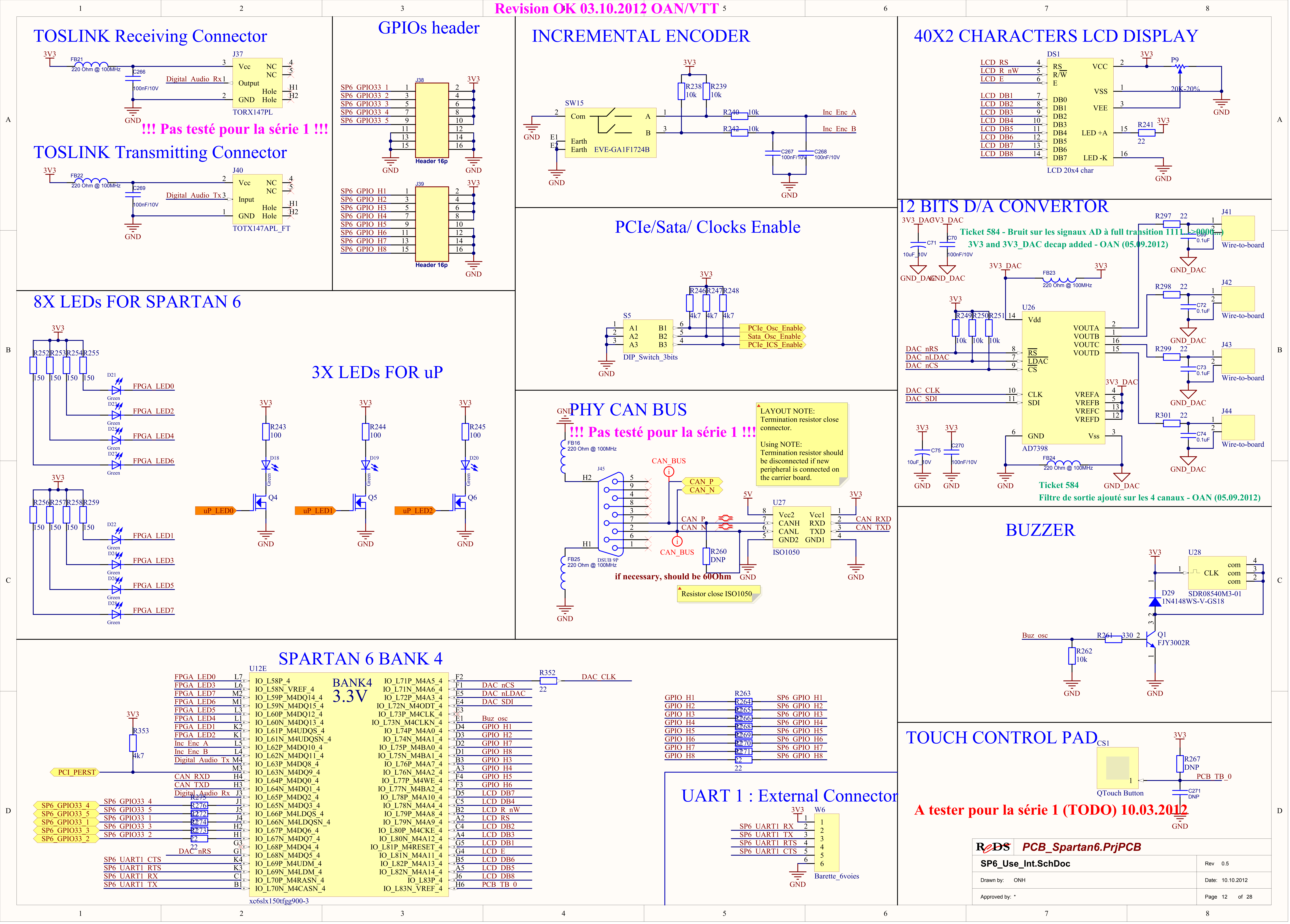
Ticket 605/613 - erreurs dues au manque de soudure sur les deux FMC
A mettre dans rapport à Locatis (TODO)

Revision OK 03.10.2012 OAN/VTT

Ticket 609 - FMC2 n'est pas compatible avec les signaux LVDS => utiliser uniquement avec des cartes FMC avec pins single-ended
A mettre dans datasheet Reptar (TODO)



PCB_Spartan6.PrjPCB		
SP6_FMC2.SchDoc		Rev 0.5
Drawn by: ONH		Date: 10.10.2012
Approved by: *		Page 11 of 28


Revision OK 03.10.2012 OAN/VTT
TOSLINK Receiving Connector
J37
TORX147PL
Digital_Audio_Rx
!!! Pas testé pour la série 1 !!!
TOSLINK Transmitting Connector
J40
TOTX147APL_FT
Digital_Audio_Tx
GPIOs header
SP6_GPIO33_1
SP6_GPIO33_2
SP6_GPIO33_3
SP6_GPIO33_4
SP6_GPIO33_5
Header 16p
SP6_GPIO_H1
SP6_GPIO_H2
SP6_GPIO_H3
SP6_GPIO_H4
SP6_GPIO_H5
SP6_GPIO_H6
SP6_GPIO_H7
SP6_GPIO_H8
INCREMENTAL ENCODER
SW15
EVE-GA1F1724B
Inc_Enc_A
Inc_Enc_B
40X2 CHARACTERS LCD DISPLAY
DS1
LCD 20x4 char
LCD_RS
LCD_R_nW
LCD_E
LCD_DB1
LCD_DB2
LCD_DB3
LCD_DB4
LCD_DB5
LCD_DB6
LCD_DB7
LCD_DB8
12 BITS D/A CONVERTOR
Ticket 584 - Bruit sur les signaux AD à full transition 1111 -> 0000...)
3V3 and 3V3_DAC decap added - OAN (05.09.2012)
U26
AD7398
DAC_nRS
DAC_nLDAC
DAC_nCS
DAC_CLK
DAC_SDI
Wire-to-board
Ticket 584
Filtre de sortie ajouté sur les 4 canaux - OAN (05.09.2012)
PCIe/Sata/ Clocks Enable
S5
DIP_Switch_3bits
PCIe_Osc_Enable
Sata_Osc_Enable
PCIe_ICS_Enable
8X LEDs FOR SPARTAN 6
FPGA_LED0
FPGA_LED2
FPGA_LED4
FPGA_LED6
FPGA_LED1
FPGA_LED3
FPGA_LED5
FPGA_LED7
3X LEDs FOR uP
uP_LED0
uP_LED1
uP_LED2
PHY CAN BUS
!!! Pas testé pour la série 1 !!!
LAYOUT NOTE:
Termination resistor close connector.
Using NOTE:
Termination resistor should be disconnected if new peripheral is connected on the carrier board.
CAN_BUS
CAN_P
CAN_N
U27
ISO1050
CAN_RXD
CAN_TXD
DSUB 9P
if necessary, should be 60Ohm
Resistor close ISO1050
BUZZER
U28
SDR08540M3-01
D29
1N4148WS-V-GS18
Q1
FJY3002R
Buz_osc
SPARTAN 6 BANK 4
U12E
BANK4
3.3V
xc6slx150tfgg900-3
PCI_PERST
DAC_CLK
SP6_UART1_CTS
SP6_UART1_RTS
SP6_UART1_RX
SP6_UART1_TX
TOUCH CONTROL PAD
CS1
QTouch Button
PCB_TB_0
A tester pour la série 1 (TODO) 10.03.2012
UART 1 : External Connector
W6
Barette_6voies
PCB_Spartan6.PrjPCB
SP6_Use_Int.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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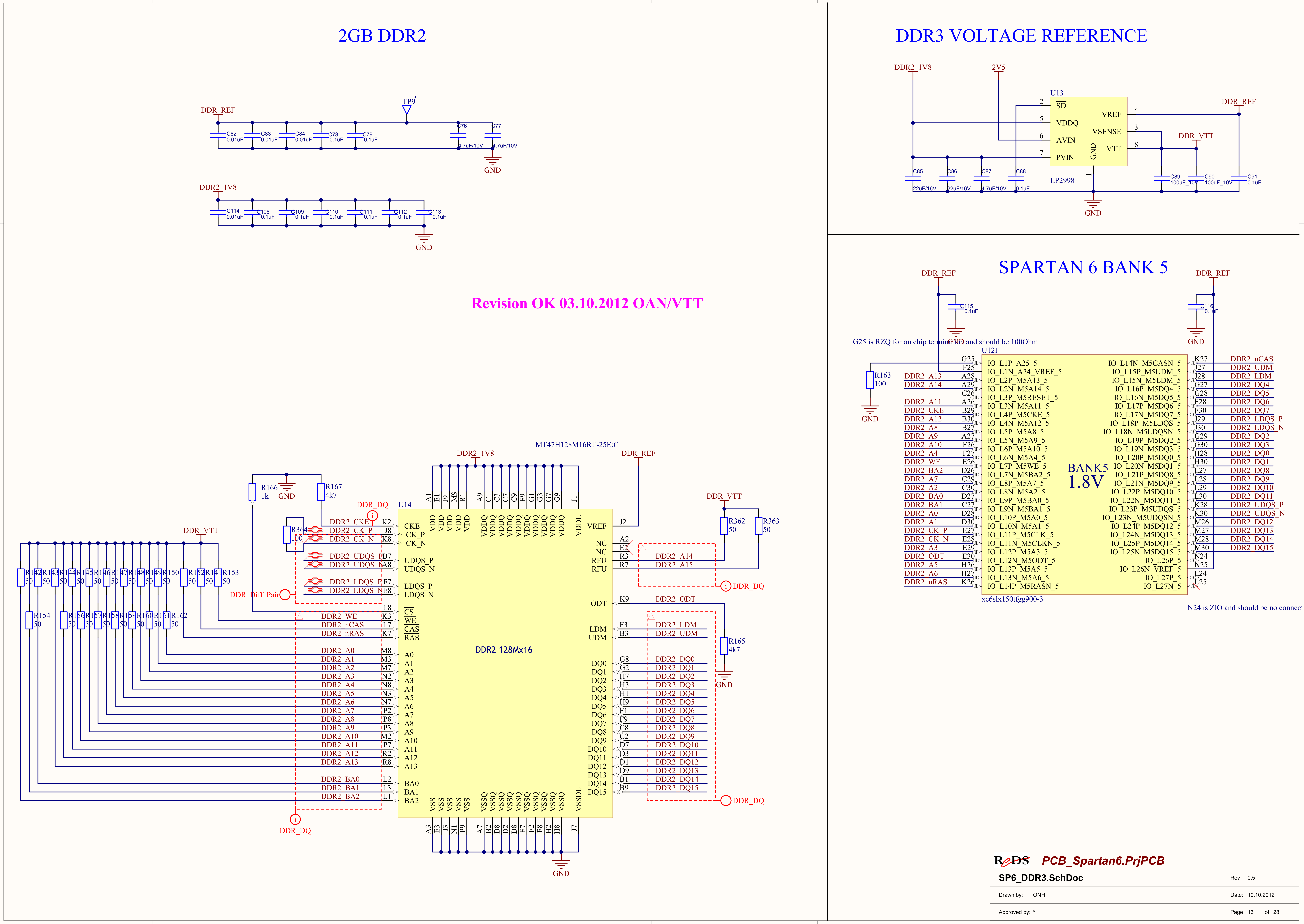

2GB DDR2
DDR3 VOLTAGE REFERENCE
SPARTAN 6 BANK 5
Revision OK 03.10.2012 OAN/VTT
DDR_REF
DDR2_1V8
DDR_VTT
2V5
GND
TP9
U13
LP2998
SD
VDDQ
AVIN
PVIN
VREF
VSENSE
VTT
U14
MT47H128M16RT-25E:C
DDR2 128Mx16
DDR_DQ
DDR_Diff_Pair
G25 is RZQ for on chip termination and should be 100Ohm
U12F
BANK5
1.8V
xc6slx150tfgg900-3
N24 is ZIO and should be no connect
PCB_Spartan6.PrjPCB
SP6_DDR3.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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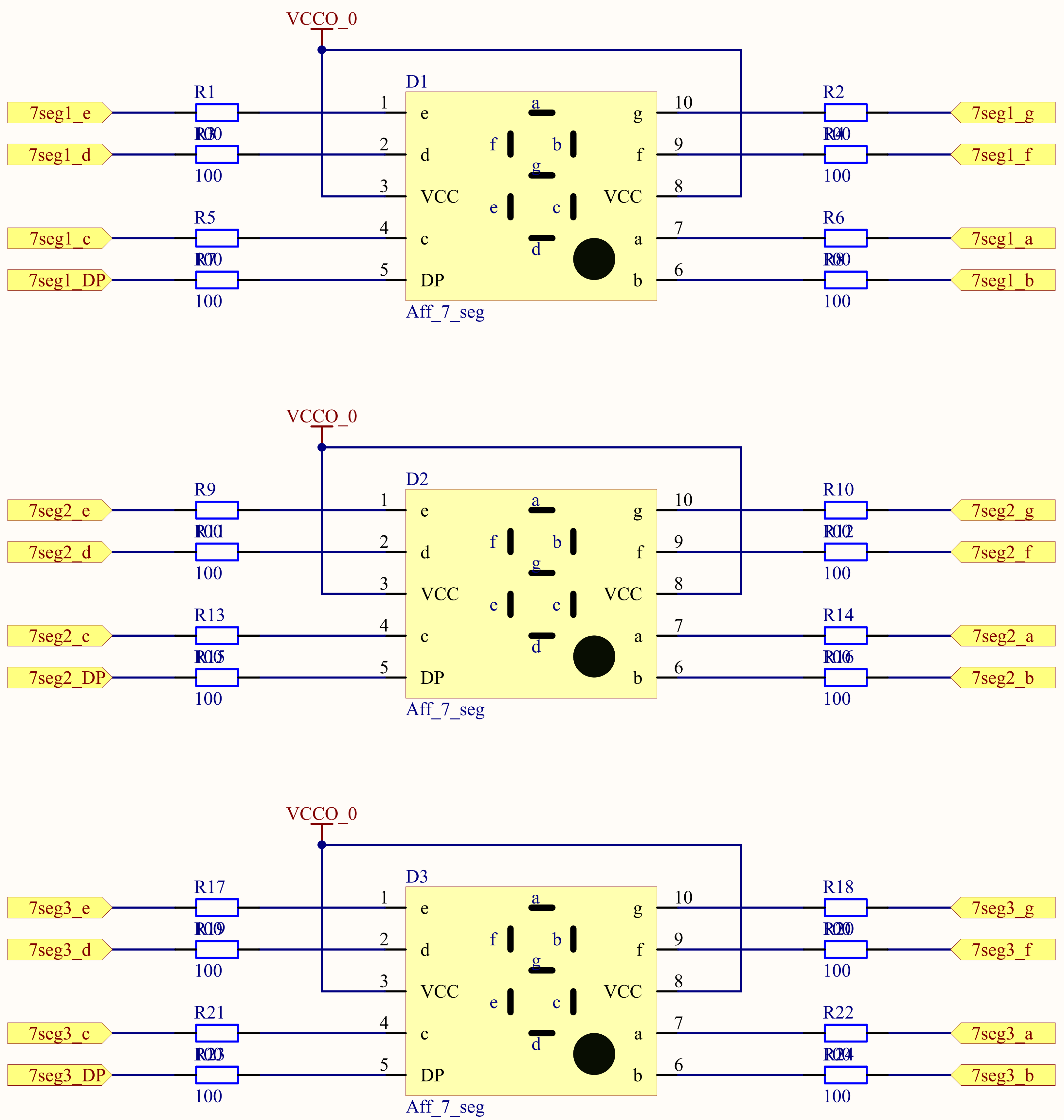
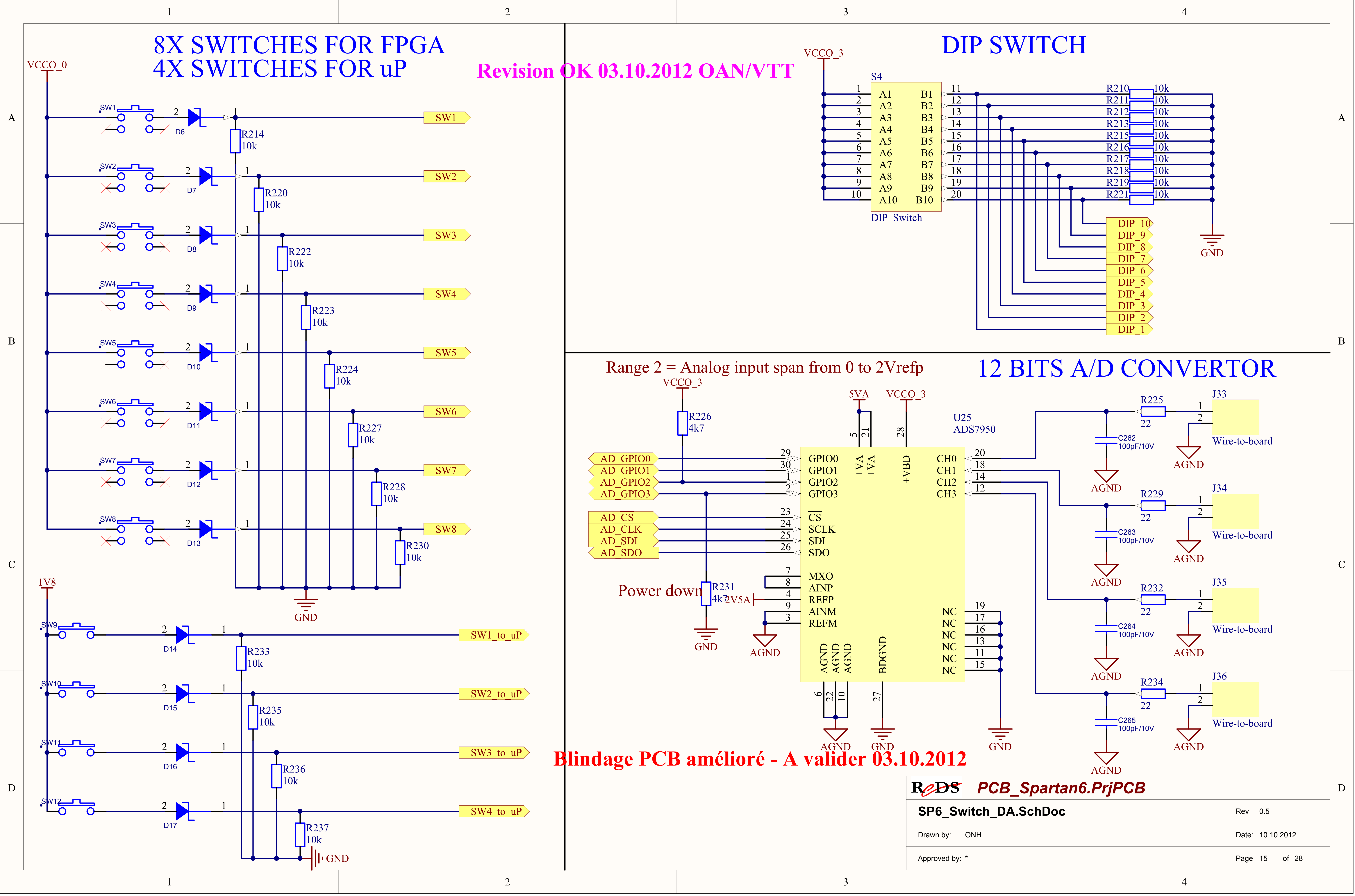
3 X 7 SEGMENTS



Revision OK 03.10.2012 OAN/VTT

VCCO_0	= 2V5/3V3
LED Vforward	= 1V8
LED Ifwd type	= 10mA => 1 luminous
Imax = 3.3-1.8/100	= 15mA => 1.4 luminous
Imax = 2.5-1.8/100	= 7mA => 0.6 luminous

ReDS **PCB_Spartan6.PrjPCB**	
SP6_7seg.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 14 of 28


8X SWITCHES FOR FPGA
4X SWITCHES FOR uP
Revision OK 03.10.2012 OAN/VTT
DIP SWITCH
VCCO_0
VCCO_3
S4
DIP_Switch
R210 R211 R212 R213 R215 R216 R217 R218 R219 R221 10k
DIP_10 DIP_9 DIP_8 DIP_7 DIP_6 DIP_5 DIP_4 DIP_3 DIP_2 DIP_1
GND
SW1 SW2 SW3 SW4 SW5 SW6 SW7 SW8
D6 D7 D8 D9 D10 D11 D12 D13
R214 R220 R222 R223 R224 R227 R228 R230 10k
1V8
SW9 SW10 SW11 SW12
D14 D15 D16 D17
R233 R235 R236 R237 10k
SW1_to_uP
SW2_to_uP
SW3_to_uP
SW4_to_uP
Range 2 = Analog input span from 0 to 2Vrefp
12 BITS A/D CONVERTOR
R226 4k7
5VA
U25
ADS7950
AD_GPIO0 AD_GPIO1 AD_GPIO2 AD_GPIO3
AD_CS AD_CLK AD_SDI AD_SDO
GPIO0 GPIO1 GPIO2 GPIO3 CS SCLK SDI SDO MXO AINP REFP AINM REFM
CH0 CH1 CH2 CH3 NC
+VA +VA +VBD AGND BDGND
Power down
R231 4k7
2V5A
AGND
R225 R229 R232 R234 22
C262 C263 C264 C265 100pF/10V
J33 J34 J35 J36
Wire-to-board
Blindage PCB amélioré - A valider 03.10.2012
PCB_Spartan6.PrjPCB
SP6_Switch_DA.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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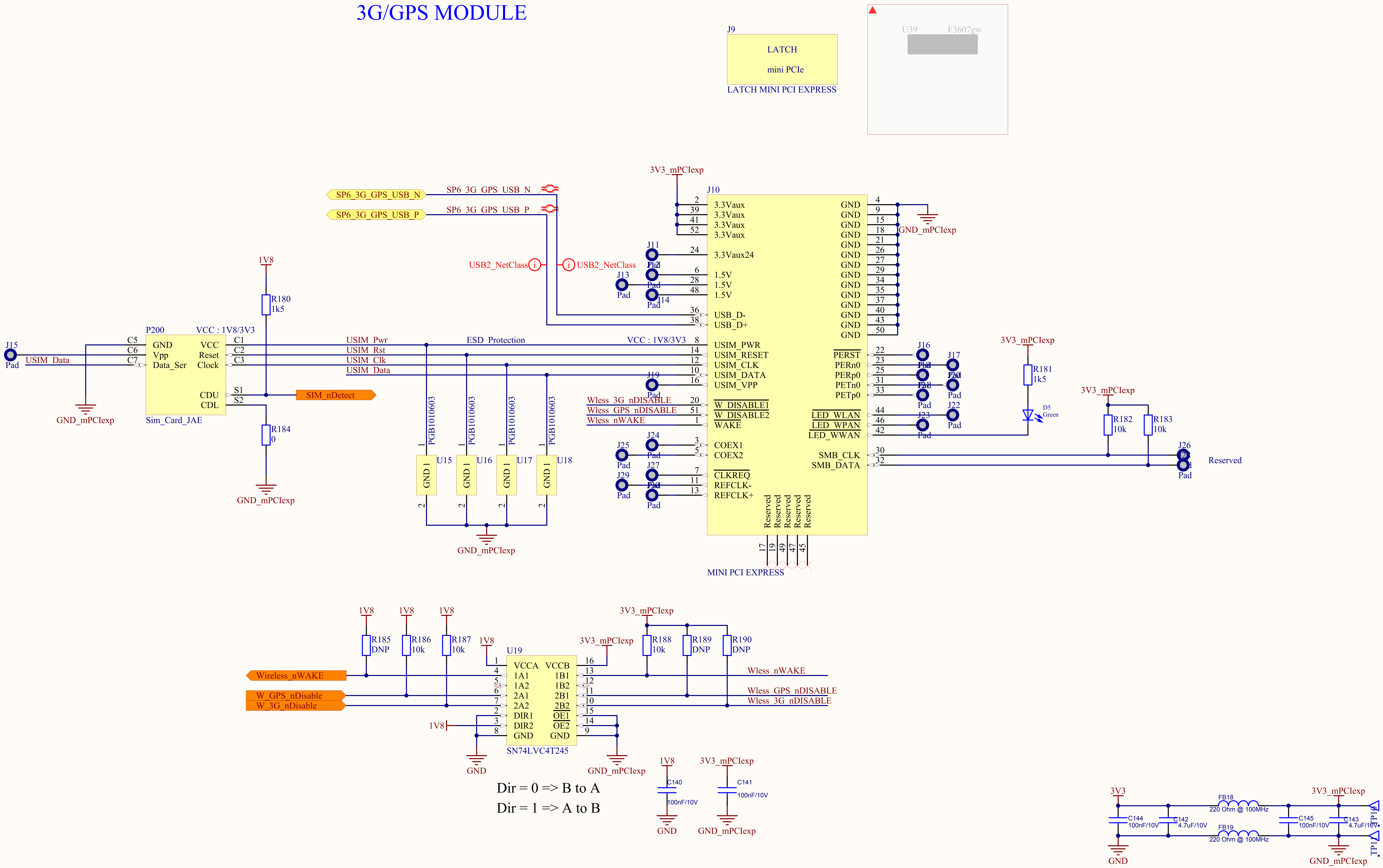
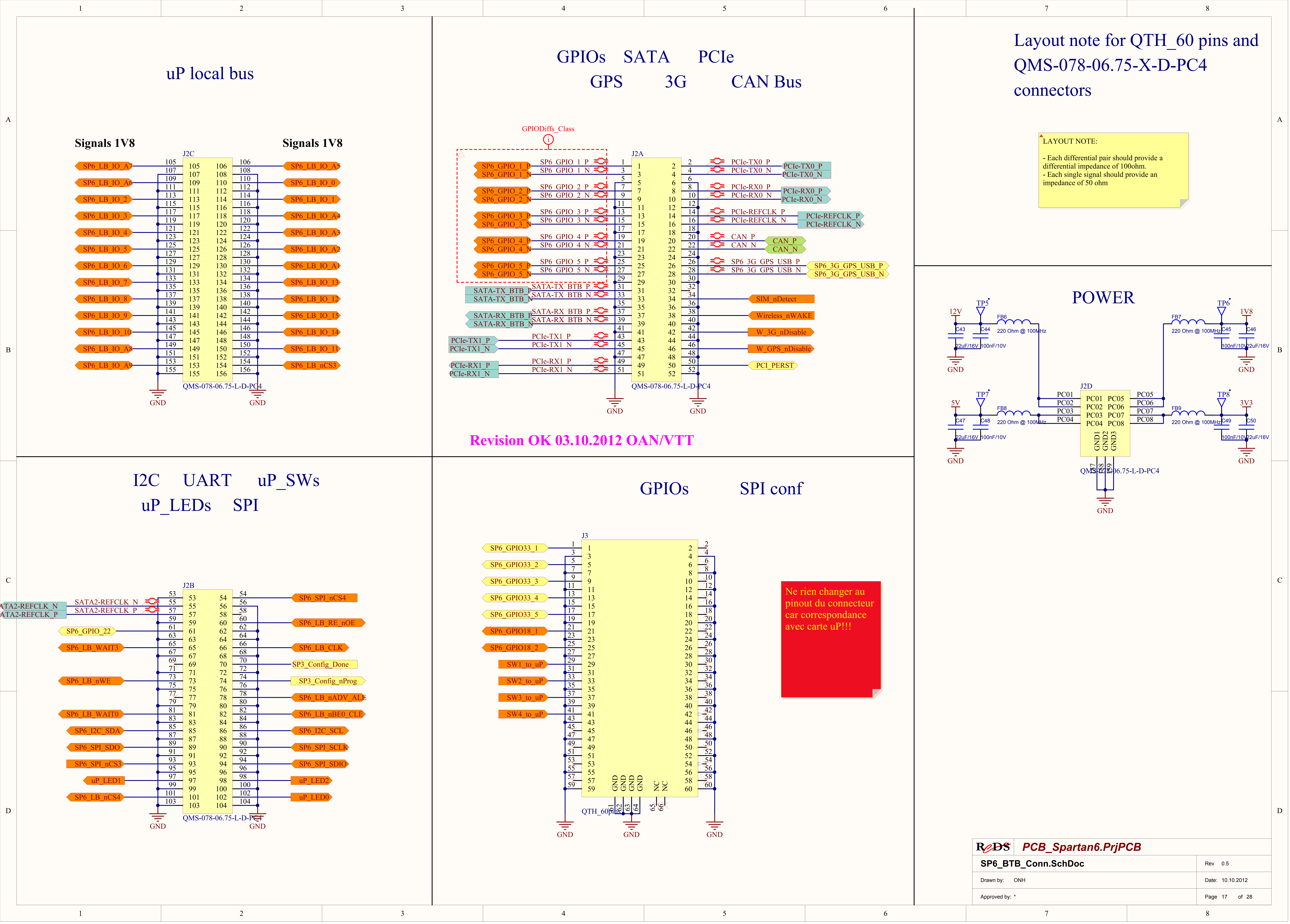
Revision OK 03.10.2012 OAN/VTT

3G/GPS MODULE



ReDS PCB_Spartan6.PrjPCB

SP6_GPS_3G.SchDoc	Rev 0.5
Drawn by: VTT	Date: 10.10.2012
Approved by: *	Page 16 of 28



uP local bus
Signals 1V8
Signals 1V8
J2C
QMS-078-06.75-L-D-PC4
GPIOs SATA PCIe
GPS 3G CAN Bus
GPIODiffs_Class
J2A
QMS-078-06.75-L-D-PC4
SIM_nDetect
Wireless_nWAKE
W_3G_nDisable
W_GPS_nDisable
PCI_PERST
Revision OK 03.10.2012 OAN/VTT
Layout note for QTH_60 pins and QMS-078-06.75-X-D-PC4 connectors
LAYOUT NOTE:
- Each differential pair should provide a differential impedance of 100ohm.
- Each single signal should provide an impedance of 50 ohm
POWER
J2D
QMS-078-06.75-L-D-PC4
220 Ohm @ 100MHz
I2C UART uP_SWs
uP_LEDs SPI
J2B
QMS-078-06.75-L-D-PC4
GPIOs SPI conf
J3
QTH_60pins
Ne rien changer au pinout du connecteur car correspondance avec carte uP!!!
GND
PCB_Spartan6.PrjPCB
SP6_BTB_Conn.SchDoc
Rev 0.5
Drawn by: ONH
Date: 10.10.2012
Approved by: *
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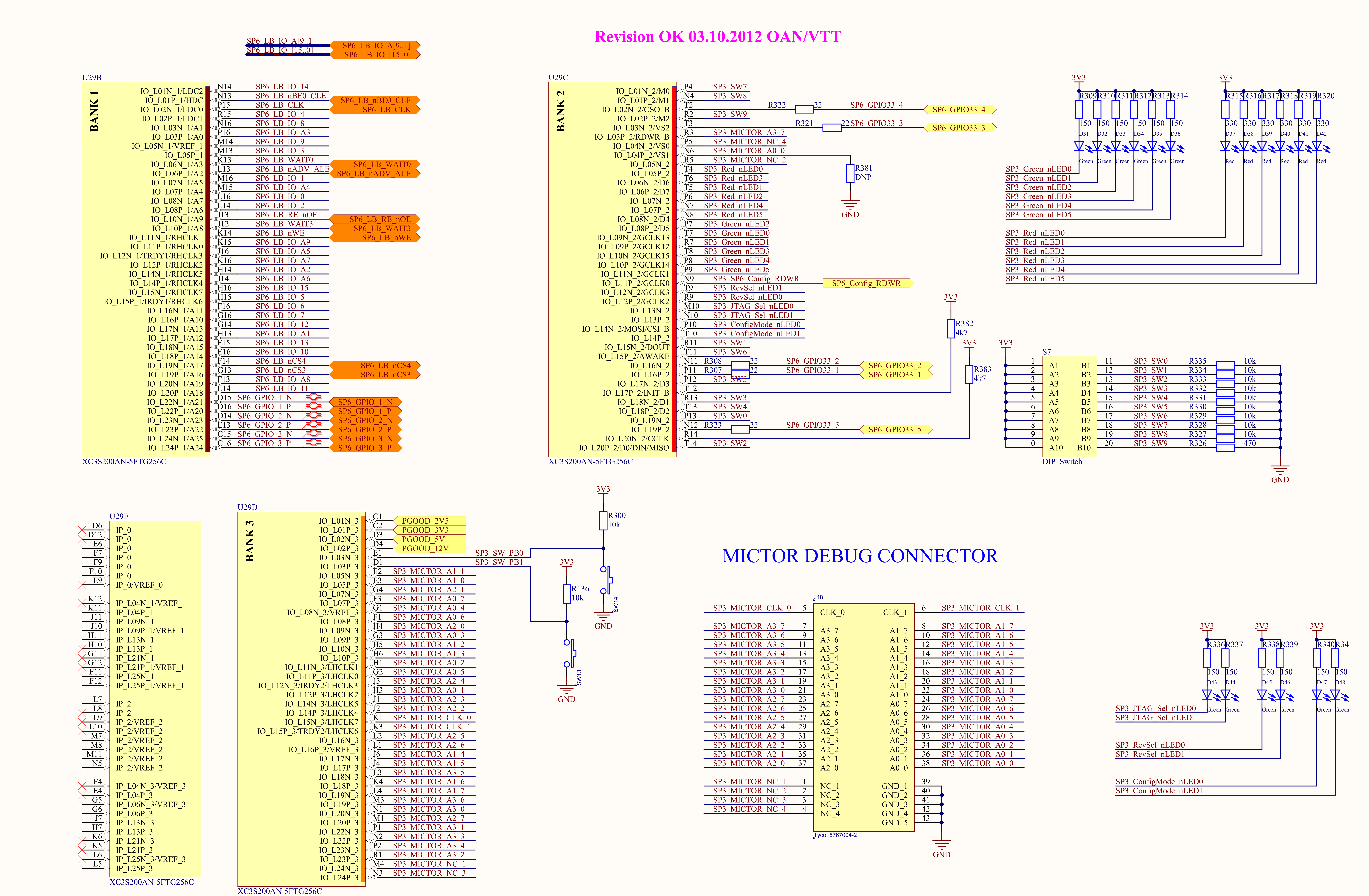
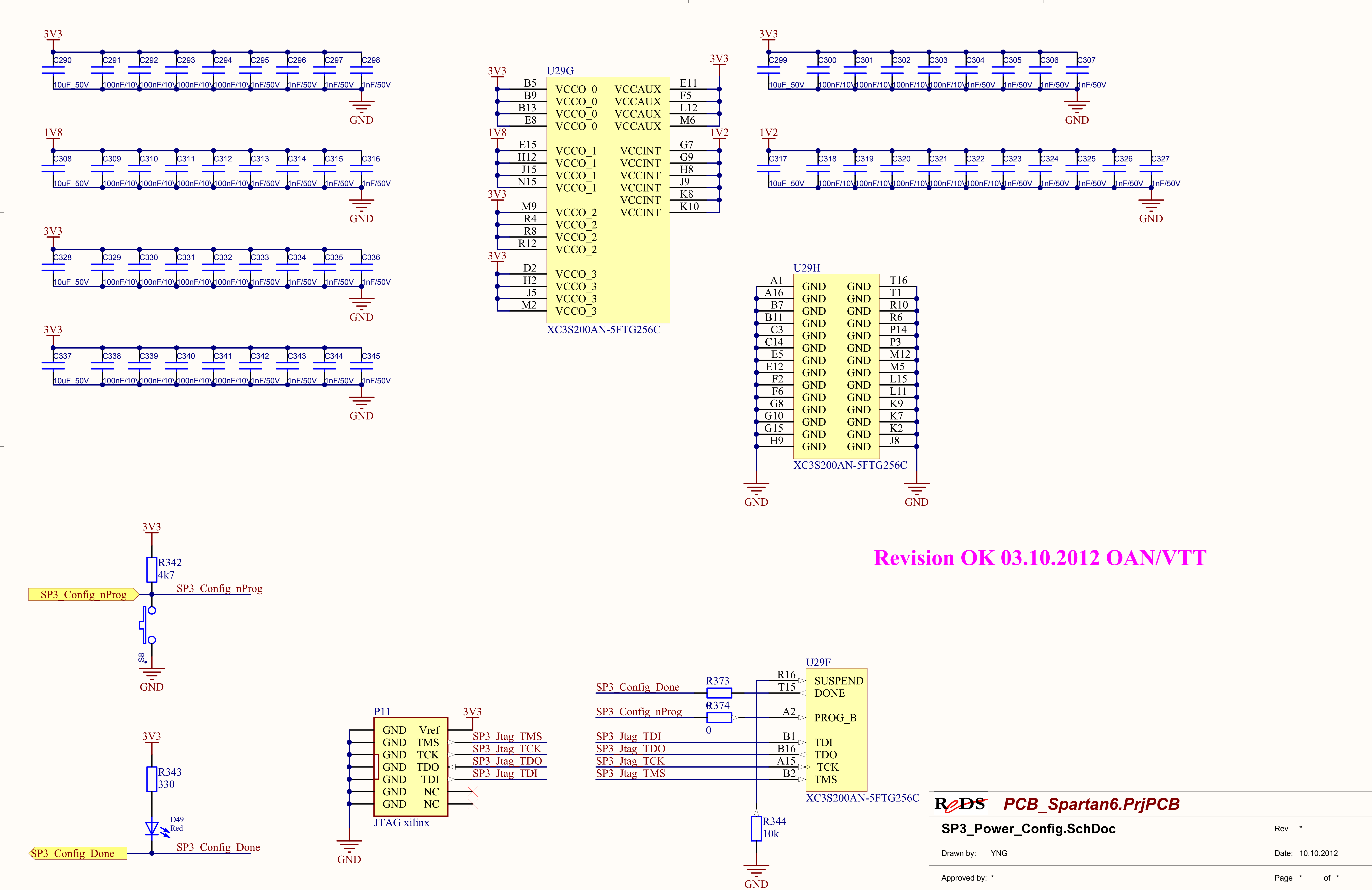
U_SP6_Jtag_Chain
SP6_Jtag_Chain.SchDoc
U_SP3_SP6_Configuration
SP3_SP6_Configuration.SchDoc
U_SP6_Conf_80pins
SP6_Conf_80pins.SchDoc
U_SP6_LB_Serial
SP6_LB_Serial.SchDoc
U_SP6_BTB_Conn
SP6_BTB_Conn.SchDoc
U_SP6_Board_Power
SP6_Board_Power.SchDoc
U_SP6_Power
SP6_Power.SchDoc
U_SP6_GTP_SMB
SP6_GTP_SMB.SchDoc
U_SP6_DDR3
SP6_DDR3.SchDoc
U_SP3_Bank1_2_3
SP3_Bank1_2_3.SchDoc
U_SP6_GPS_3G
SP6_GPS_3G.SchDoc
U_SP6_PCIe
SP6_PCIe.SchDoc
U_SP6_SATA
SP6_SATA.SchDoc
U_SP6_Use_Int
SP6_Use_Int.SchDoc
U_SP6_FMC2
SP6_FMC2.SchDoc
U_SP6_Switch_DA
SP6_Switch_DA.SchDoc
U_SP6_FMC1
SP6_FMC1.SchDoc
U_SP6_7seg
SP6_7seg.SchDoc
U_SP3_Power_Config
SP3_Power_Config.SchDoc
U37
U38
FPGA_board_Production
FPGA_PCB
GND
Revision OK 03.10.2012 OAN/VTT
PCB_Spartan6.PrjPCB
FPGA_Board.SchDoc
Drawn by: YNG/VTT
Date: 10.10.2012
Approved by: *
Rev *
Page * of *



ReDS	PCB_Spartan6.PrjPCB		
SP3_Bank1_2_3.SchDoc		Rev *	
Drawn by: YNG		Date: 10.10.2012	
Approved by: *		Page *	of *



3V3
C290 C291 C292 C293 C294 C295 C296 C297 C298
10uF 50V 100nF/10V 100nF/10V 100nF/10V 100nF/10V 1nF/50V 1nF/50V 1nF/50V 1nF/50V
GND
1V8
C308 C309 C310 C311 C312 C313 C314 C315 C316
3V3
C328 C329 C330 C331 C332 C333 C334 C335 C336
3V3
C337 C338 C339 C340 C341 C342 C343 C344 C345
U29G
B5 B9 B13 E8 VCCO_0
E15 H12 J15 N15 VCCO_1
M9 R4 R8 R12 VCCO_2
D2 H2 J5 M2 VCCO_3
VCCAUX E11 F5 L12 M6
1V2
VCCINT G7 G9 H8 J9 K8 K10
XC3S200AN-5FTG256C
3V3
C299 C300 C301 C302 C303 C304 C305 C306 C307
1V2
C317 C318 C319 C320 C321 C322 C323 C324 C325 C326 C327
U29H
A1 A16 B7 B11 C3 C14 E5 E12 F2 F6 G8 G10 G15 H9
T16 T1 R10 R6 P14 P3 M12 M5 L15 L11 K9 K7 K2 J8
GND
XC3S200AN-5FTG256C
Revision OK 03.10.2012 OAN/VTT
R342
4k7
SP3_Config_nProg
S8
R343
330
D49
Red
SP3_Config_Done
P11
GND Vref
GND TMS
GND TCK
GND TDO
GND TDI
GND NC
GND NC
JTAG xilinx
SP3_Jtag_TMS
SP3_Jtag_TCK
SP3_Jtag_TDO
SP3_Jtag_TDI
U29F
R373
R374
0
R16 SUSPEND
T15 DONE
A2 PROG_B
B1 TDI
B16 TDO
A15 TCK
B2 TMS
XC3S200AN-5FTG256C
R344
10k
ReDS
PCB_Spartan6.PrjPCB
SP3_Power_Config.SchDoc
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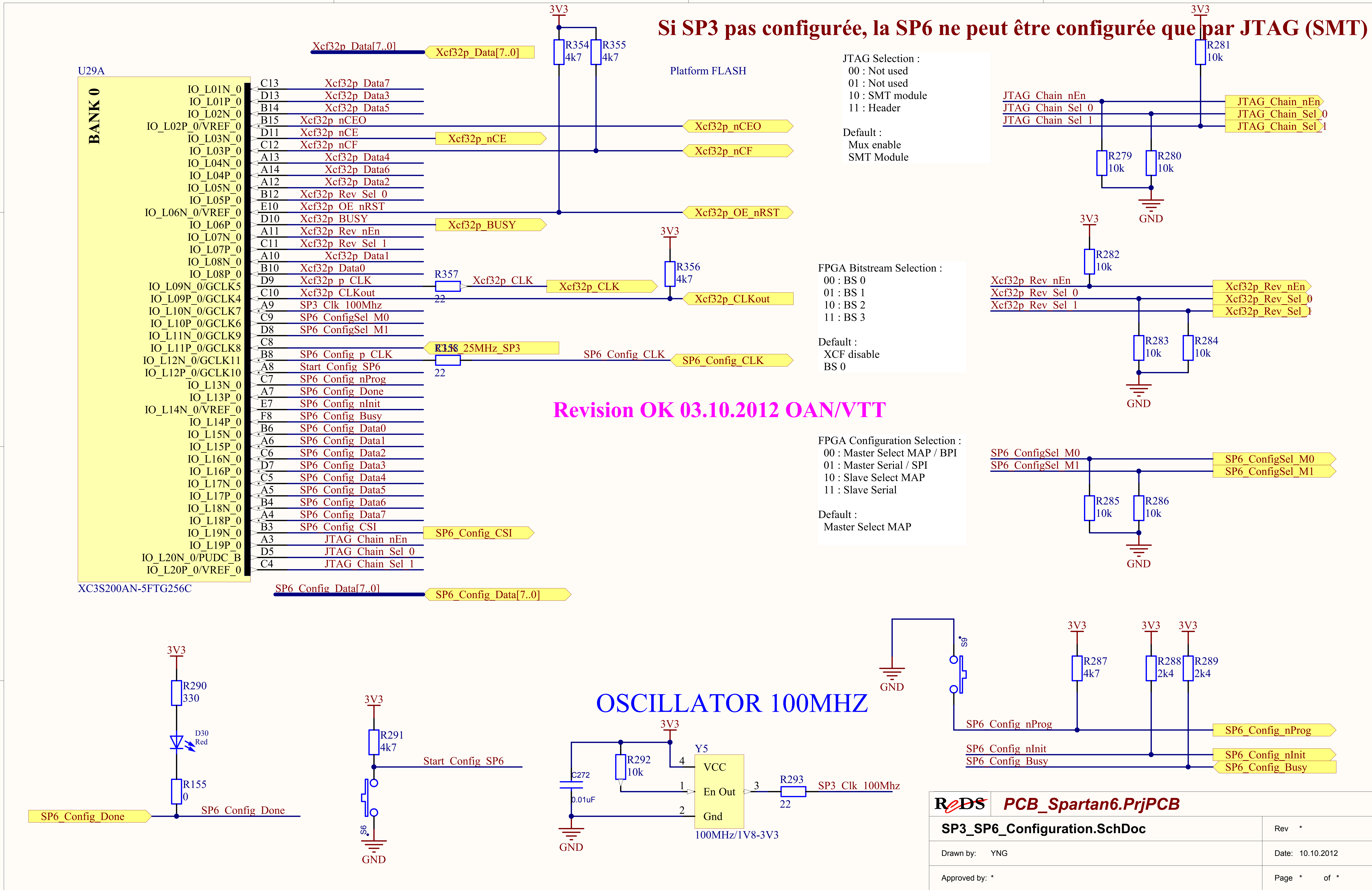

Si SP3 pas configurée, la SP6 ne peut être configurée que par JTAG (SMT)
U29A
BANK 0
IO_L01N_0
IO_L01P_0
IO_L02N_0
IO_L02P_0/VREF_0
IO_L03N_0
IO_L03P_0
IO_L04N_0
IO_L04P_0
IO_L05N_0
IO_L05P_0
IO_L06N_0/VREF_0
IO_L06P_0
IO_L07N_0
IO_L07P_0
IO_L08N_0
IO_L08P_0
IO_L09N_0/GCLK5
IO_L09P_0/GCLK4
IO_L10N_0/GCLK7
IO_L10P_0/GCLK6
IO_L11N_0/GCLK9
IO_L11P_0/GCLK8
IO_L12N_0/GCLK11
IO_L12P_0/GCLK10
IO_L13N_0
IO_L13P_0
IO_L14N_0/VREF_0
IO_L14P_0
IO_L15N_0
IO_L15P_0
IO_L16N_0
IO_L16P_0
IO_L17N_0
IO_L17P_0
IO_L18N_0
IO_L18P_0
IO_L19N_0
IO_L19P_0
IO_L20N_0/PUDC_B
IO_L20P_0/VREF_0
XC3S200AN-5FTG256C
C13 Xcf32p_Data7
D13 Xcf32p_Data3
B14 Xcf32p_Data5
B15 Xcf32p_nCEO
D11 Xcf32p_nCE
C12 Xcf32p_nCF
A13 Xcf32p_Data4
A14 Xcf32p_Data6
A12 Xcf32p_Data2
B12 Xcf32p_Rev_Sel_0
E10 Xcf32p_OE_nRST
D10 Xcf32p_BUSY
A11 Xcf32p_Rev_nEn
C11 Xcf32p_Rev_Sel_1
A10 Xcf32p_Data1
B10 Xcf32p_Data0
D9 Xcf32p_p_CLK
C10 Xcf32p_CLKout
A9 SP3_Clk_100Mhz
C9 SP6_ConfigSel_M0
D8 SP6_ConfigSel_M1
C8 CLK_25MHz_SP3
B8 SP6_Config_p_CLK
A8 Start_Config_SP6
C7 SP6_Config_nProg
A7 SP6_Config_Done
E7 SP6_Config_nInit
F8 SP6_Config_Busy
B6 SP6_Config_Data0
A6 SP6_Config_Data1
C6 SP6_Config_Data2
D7 SP6_Config_Data3
C5 SP6_Config_Data4
A5 SP6_Config_Data5
B4 SP6_Config_Data6
A4 SP6_Config_Data7
B3 SP6_Config_CSI
A3 JTAG_Chain_nEn
D5 JTAG_Chain_Sel_0
C4 JTAG_Chain_Sel_1
Xcf32p_Data[7..0]
SP6_Config_Data[7..0]
3V3
R354 4k7
R355 4k7
R356 4k7
R357 22
R358 22
Xcf32p_CLK
SP6_Config_CLK
Xcf32p_nCEO
Xcf32p_nCE
Xcf32p_nCF
Xcf32p_OE_nRST
Xcf32p_BUSY
Xcf32p_CLKout
SP6_Config_CSI
Platform FLASH
JTAG Selection :
00 : Not used
01 : Not used
10 : SMT module
11 : Header
Default :
Mux enable
SMT Module
R281 10k
R279 10k
R280 10k
JTAG_Chain_nEn
JTAG_Chain_Sel_0
JTAG_Chain_Sel_1
GND
FPGA Bitstream Selection :
00 : BS 0
01 : BS 1
10 : BS 2
11 : BS 3
Default :
XCF disable
BS 0
R282 10k
R283 10k
R284 10k
Xcf32p_Rev_nEn
Xcf32p_Rev_Sel_0
Xcf32p_Rev_Sel_1
Revision OK 03.10.2012 OAN/VTT
FPGA Configuration Selection :
00 : Master Select MAP / BPI
01 : Master Serial / SPI
10 : Slave Select MAP
11 : Slave Serial
Default :
Master Select MAP
SP6_ConfigSel_M0
SP6_ConfigSel_M1
R285 10k
R286 10k
S9
R287 4k7
R288 2k4
R289 2k4
SP6_Config_nProg
SP6_Config_nInit
SP6_Config_Busy
OSCILLATOR 100MHZ
R290 330
D30 Red
R155 0
SP6_Config_Done
R291 4k7
Start_Config_SP6
S6
C272 0.01uF
R292 10k
Y5
VCC
En Out
Gnd
100MHz/1V8-3V3
R293 22
SP3_Clk_100Mhz
PCB_Spartan6.PrjPCB
SP3_SP6_Configuration.SchDoc
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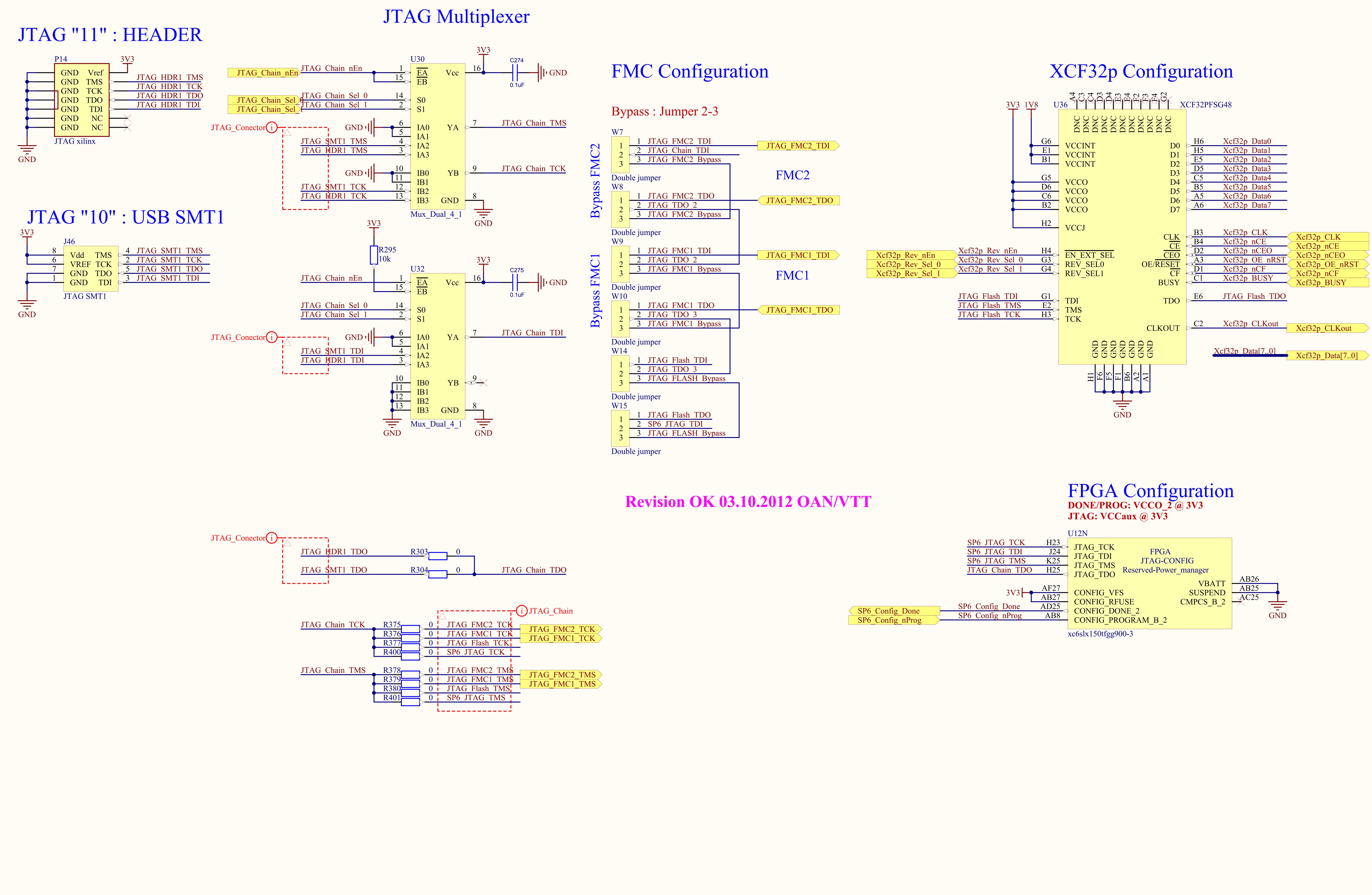

ReDS PCB_Spartan6.PrjPCB

SP6_Jtag_Chain.SchDoc

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