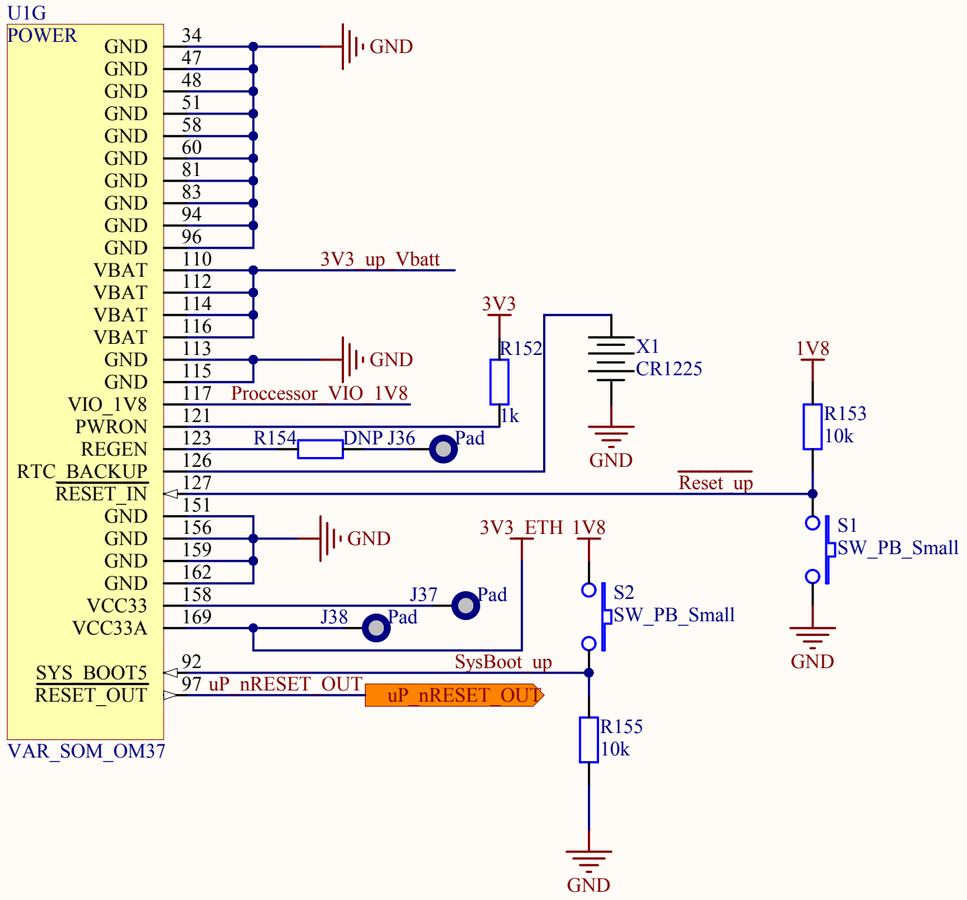
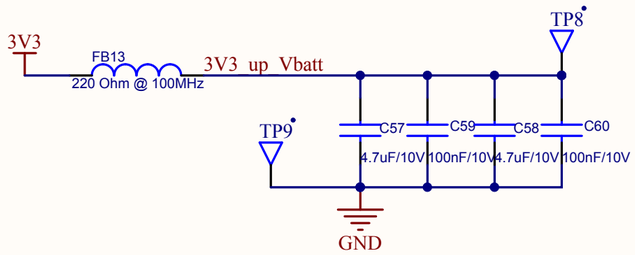
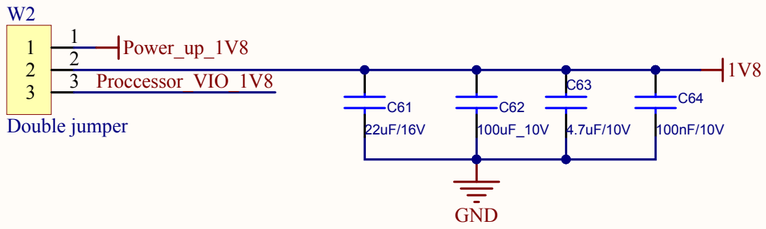
Revision OK 03.10.2012 OAN/VTT



3V3 processor voltage

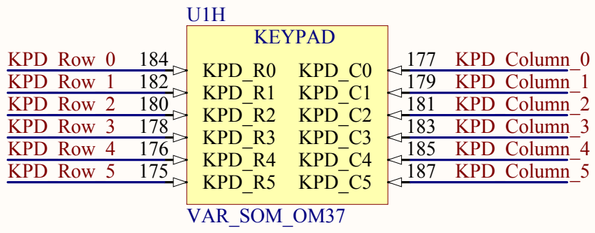


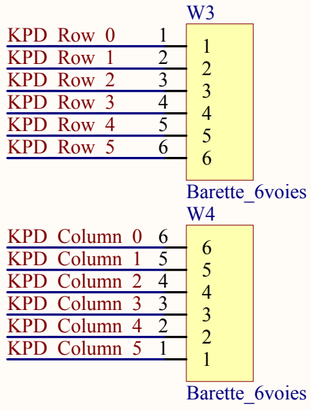
1V8 proccesor board source voltage selection



Question (03.10.2012)
Est-il nécessaire de garder cette fonctionnalité ?

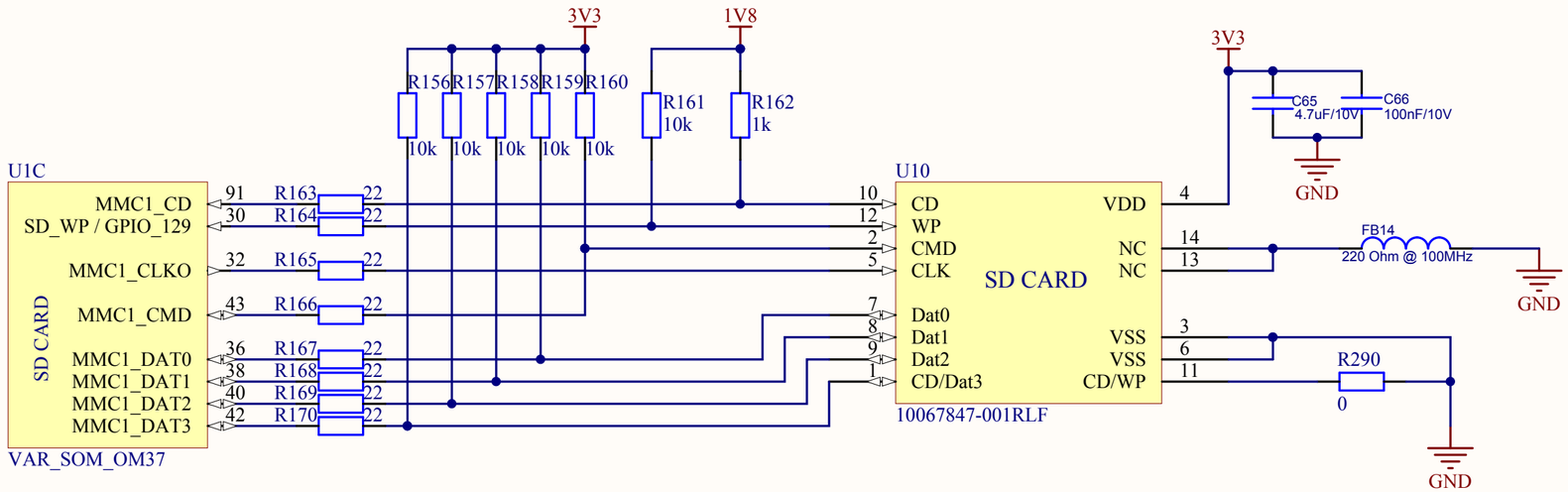
Reserved function



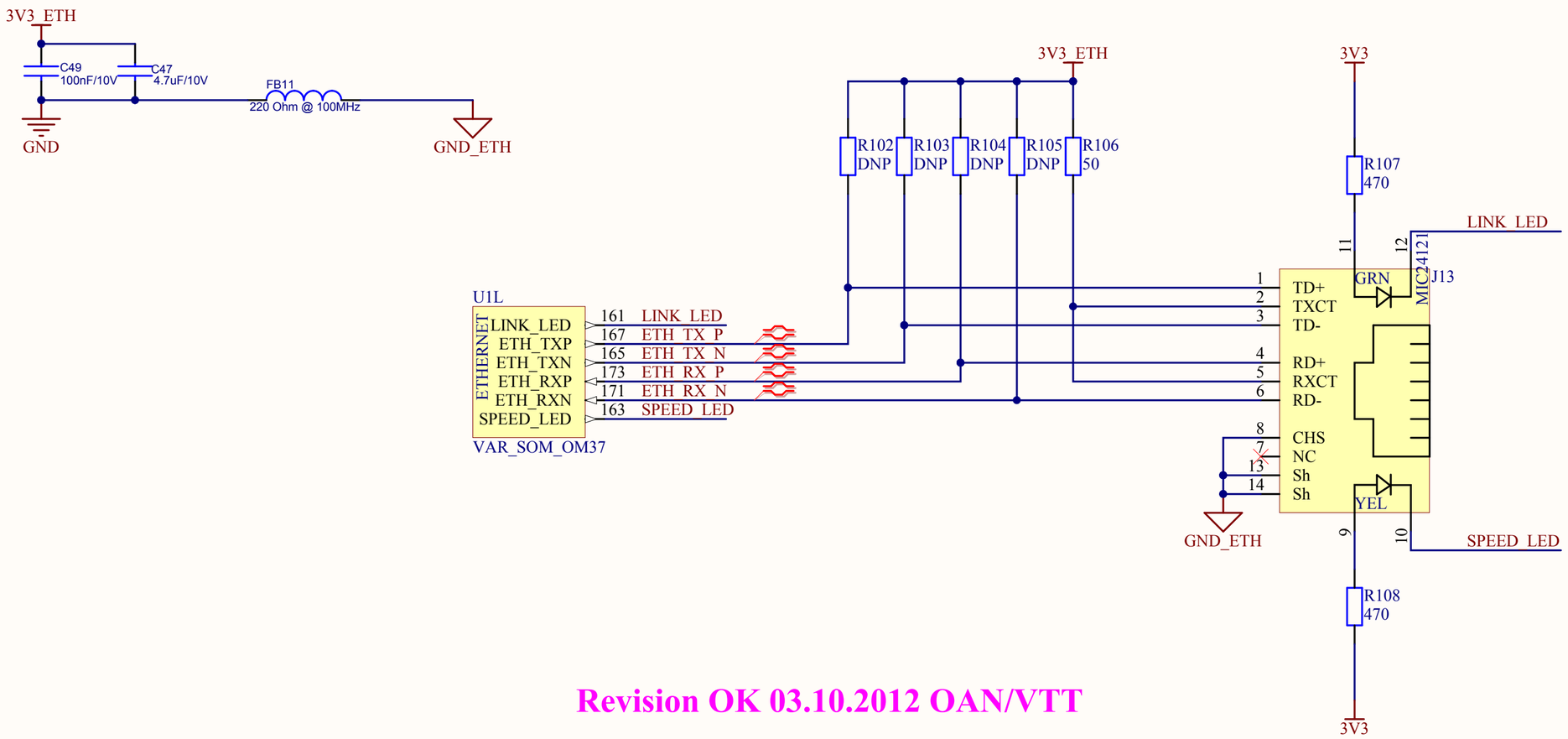


R&DS PCB_DM3730.PrjPCB	
DM3730_POWER.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 18 of 28

Revision OK 03.10.2012 OAN/VTT



R⌀DS PCB_DM3730.PrjPCB	
DM3730_SDCARD.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 19 of 28



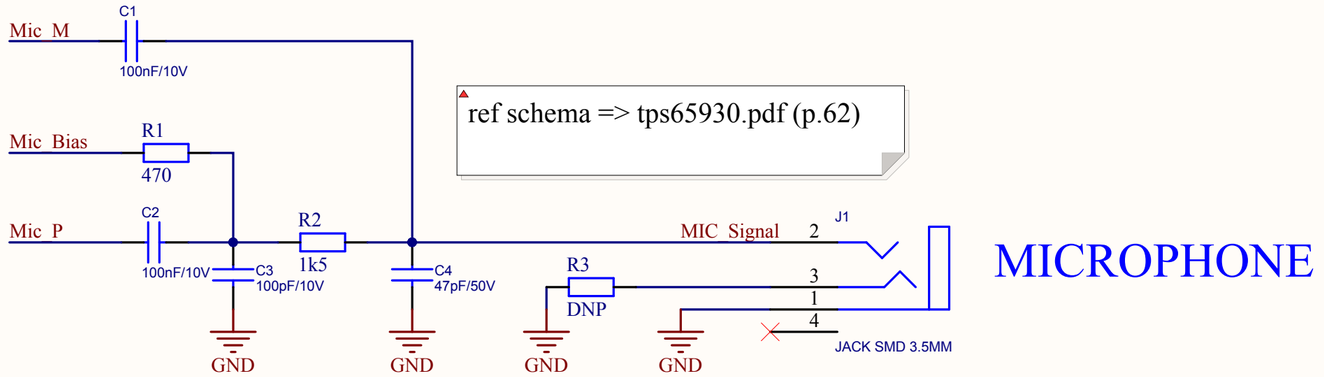
Revision OK 03.10.2012 OAN/VTT

R&DS PCB_DM3730.PrjPCB	
DM3730_ETHERNET.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 20 of 28

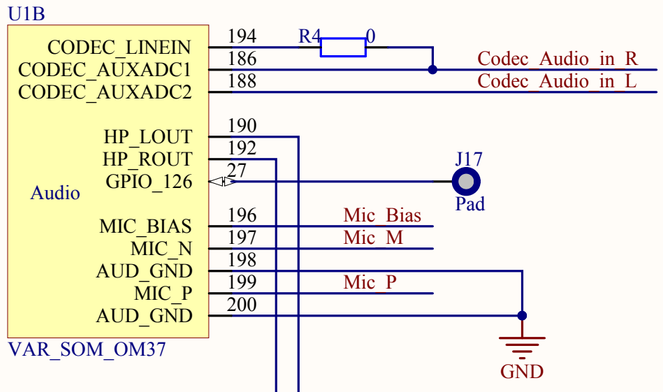
Revision OK 03.10.2012 OAN/VTT

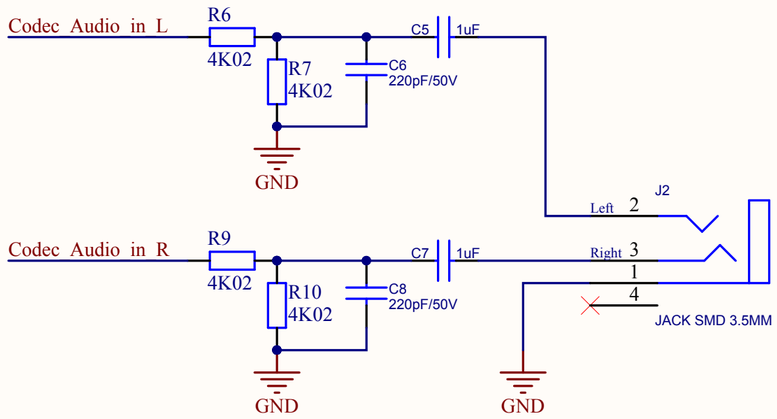
Note:

Le blindage du chemin MIC et AUDIO IN a été amélioré au niveau du PCB - A valider

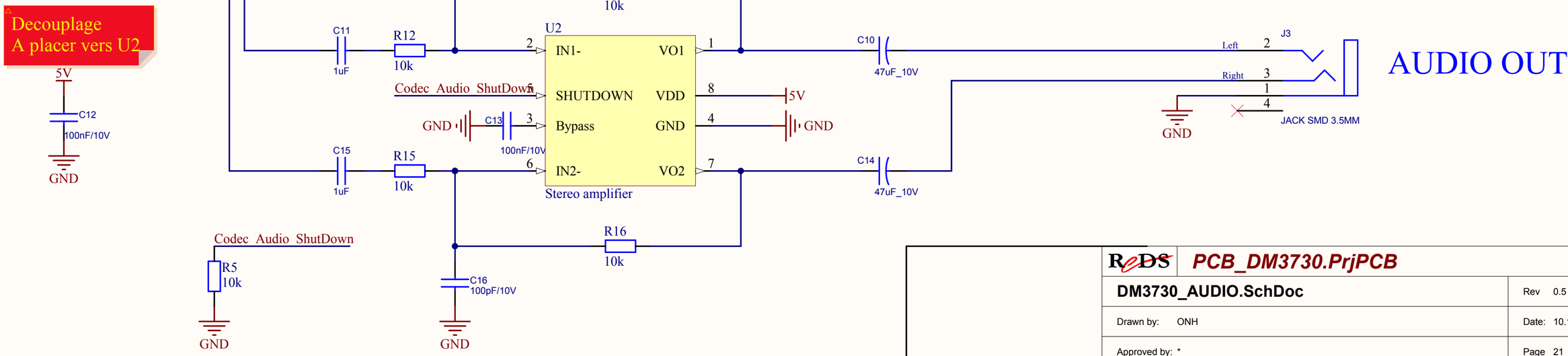


MICROPHONE





AUDIO IN

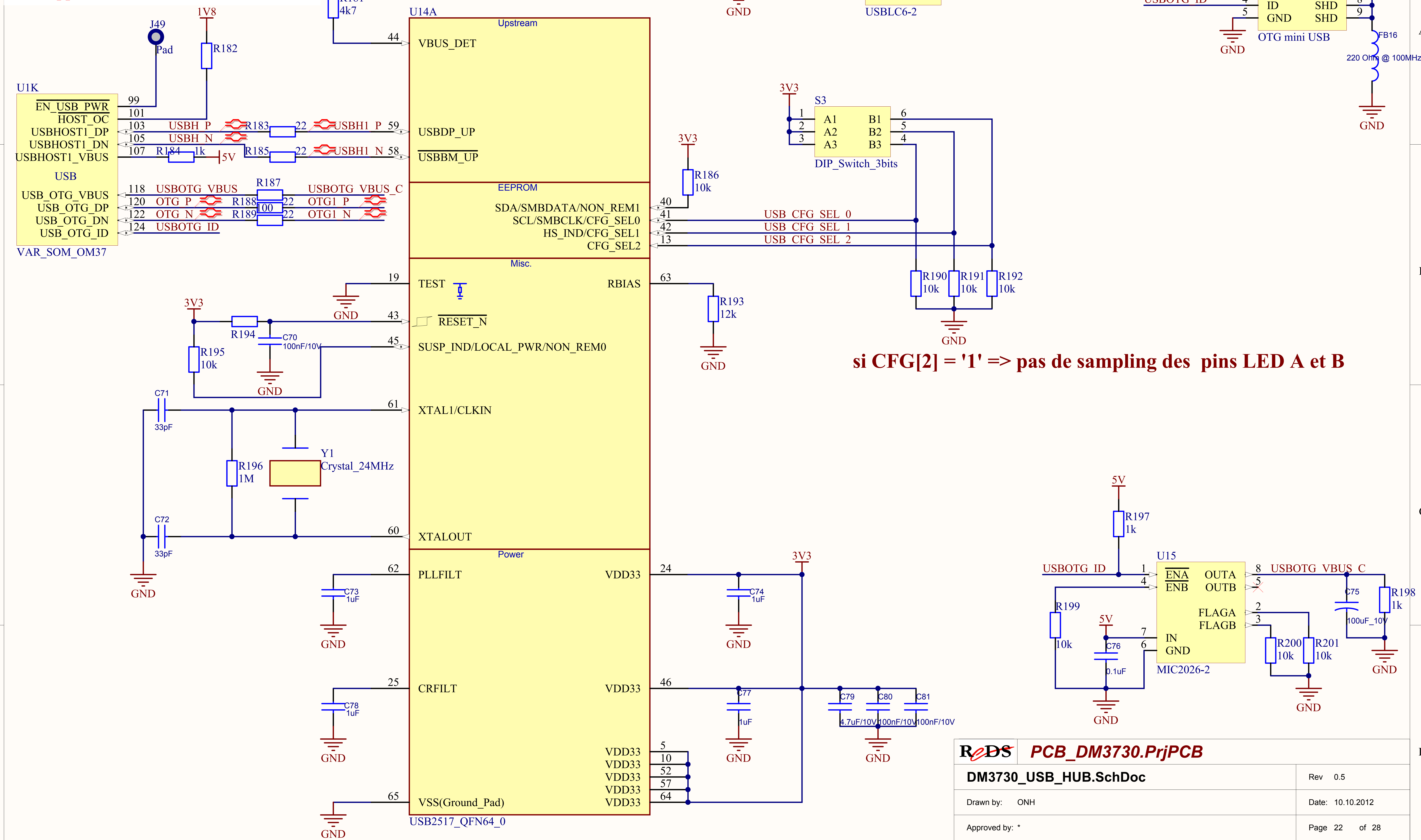


AUDIO OUT

R~~e~~DS PCB_DM3730.PrjPCB	
DM3730_AUDIO.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 21 of 28

NOTE: OTG fonctionne en mode Device - Testé et validé. En mode Master, pas validé et fonctionnalité supprimée des spec.
=> A supprimer dans Datasheet

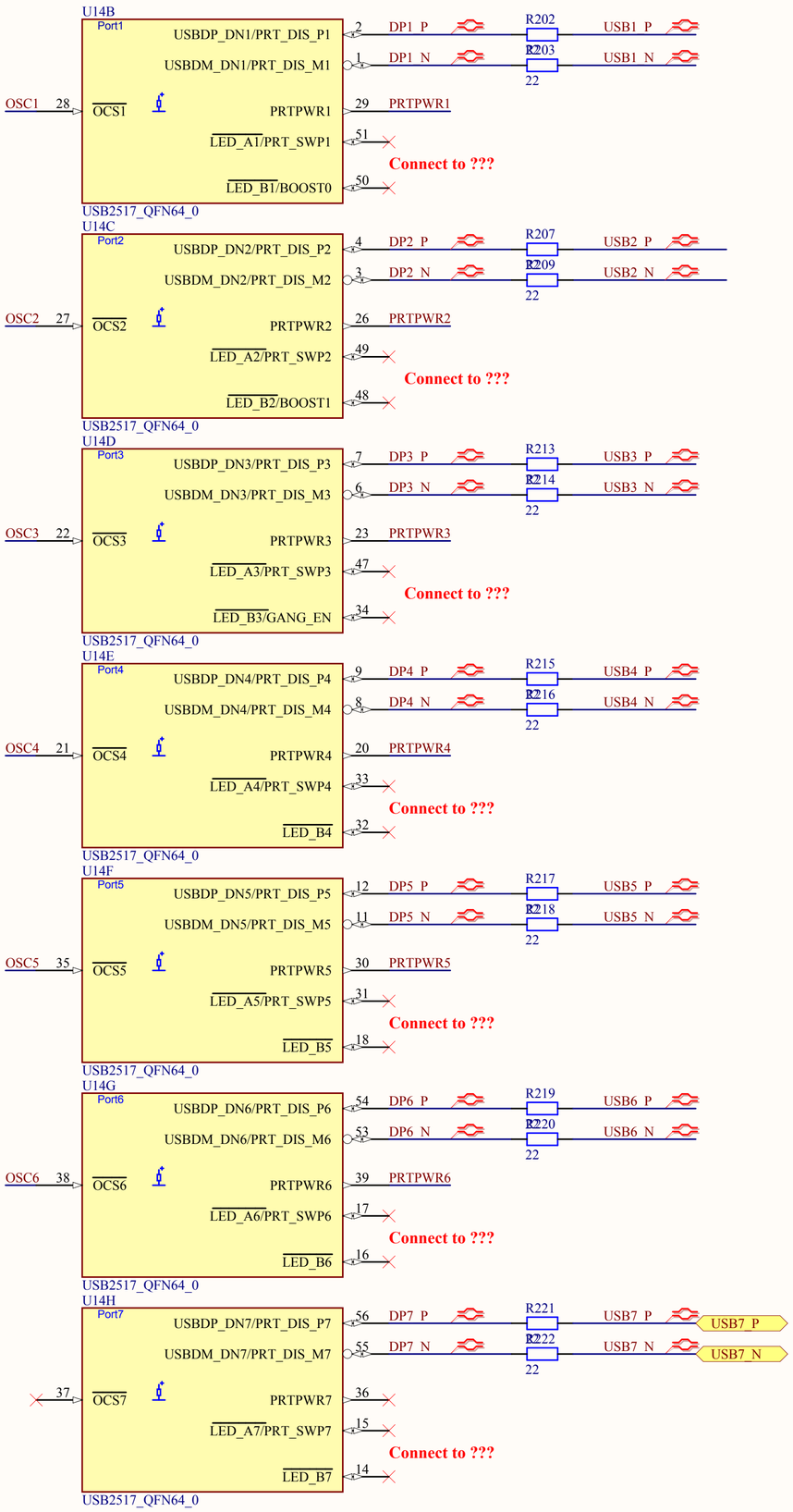
Revision OK 03.10.2012 OAN/VTT



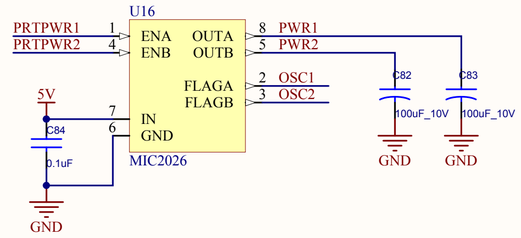
U1K
EN_USB_PWR
HOST_OC
USBHOST1_DP
USBHOST1_DN
USBHOST1_VBUS
USB
USB_OTG_VBUS
USB_OTG_DP
USB_OTG_DN
USB_OTG_ID
VAR_SOM_OM37
J49
Pad
1V8
R182
3V3
R181
4k7
U14A
Upstream
VBUS_DET
USBDP_UP
USBBM_UP
EEPROM
SDA/SMBDATA/NON_REM1
SCL/SMBCLK/CFG_SEL0
HS_IND/CFG_SEL1
CFG_SEL2
Misc.
TEST
RBIAS
RESET_N
SUSP_IND/LOCAL_PWR/NON_REM0
XTAL1/CLKIN
XTALOUT
Power
PLLFILT
CRFILT
VDD33
VSS(Ground_Pad)
USB2517_QFN64_0
USBH_P
USBH_N
R183
R184
R185
USBH1_P
USBH1_N
5V
USBOTG_VBUS
R187
USBOTG_VBUS_C
OTG_P
OTG_N
R188
R189
100
OTG1_P
OTG1_N
USBOTG_ID
R194
C70
100nF/10V
R195
10k
GND
C71
33pF
C72
33pF
R196
1M
Y1
Crystal_24MHz
C73
1uF
C78
1uF
C74
1uF
C77
1uF
C79
C80
C81
4.7uF/10V
100nF/10V
100nF/10V
U13
I/O1
GND
VBUS
I/O2
USBLC6-2
USBOTG_P
USBOTG_N
J48
VBUS
D-
D+ OTG
ID
GND
SHD
OTG mini USB
FB16
220 Ohm @ 100MHz
S3
A1
A2
A3
B1
B2
B3
DIP_Switch_3bits
R186
10k
USB_CFG_SEL_0
USB_CFG_SEL_1
USB_CFG_SEL_2
R190
R191
R192
R193
12k
si CFG[2] = '1' => pas de sampling des pins LED A et B
R197
1k
U15
ENA
ENB
OUTA
OUTB
FLAGA
FLAGB
IN
MIC2026-2
R198
1k
C75
100uF_10V
R199
C76
0.1uF
R200
R201

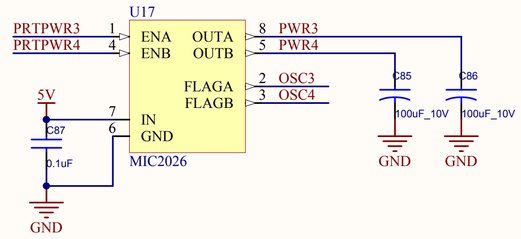
ReDS PCB_DM3730.PrjPCB

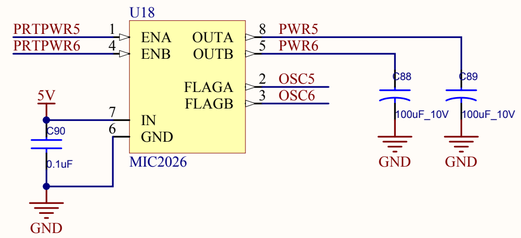
DM3730_USB_HUB.SchDoc	Rev 0.5	
Drawn by: ONH	Date: 10.10.2012	
Approved by: *	Page 22	of 28



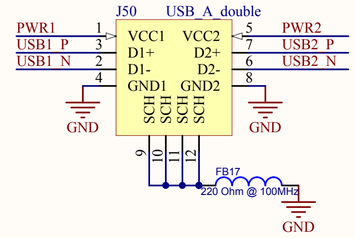
USB protection

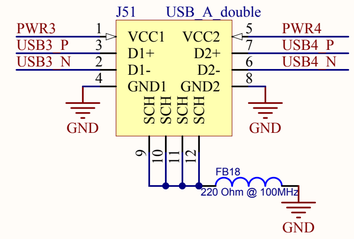


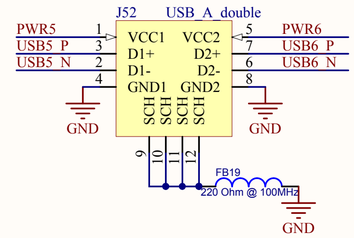




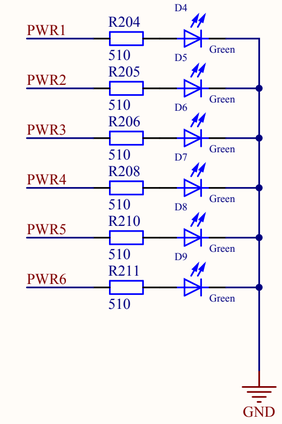
USB connectors







USB power info



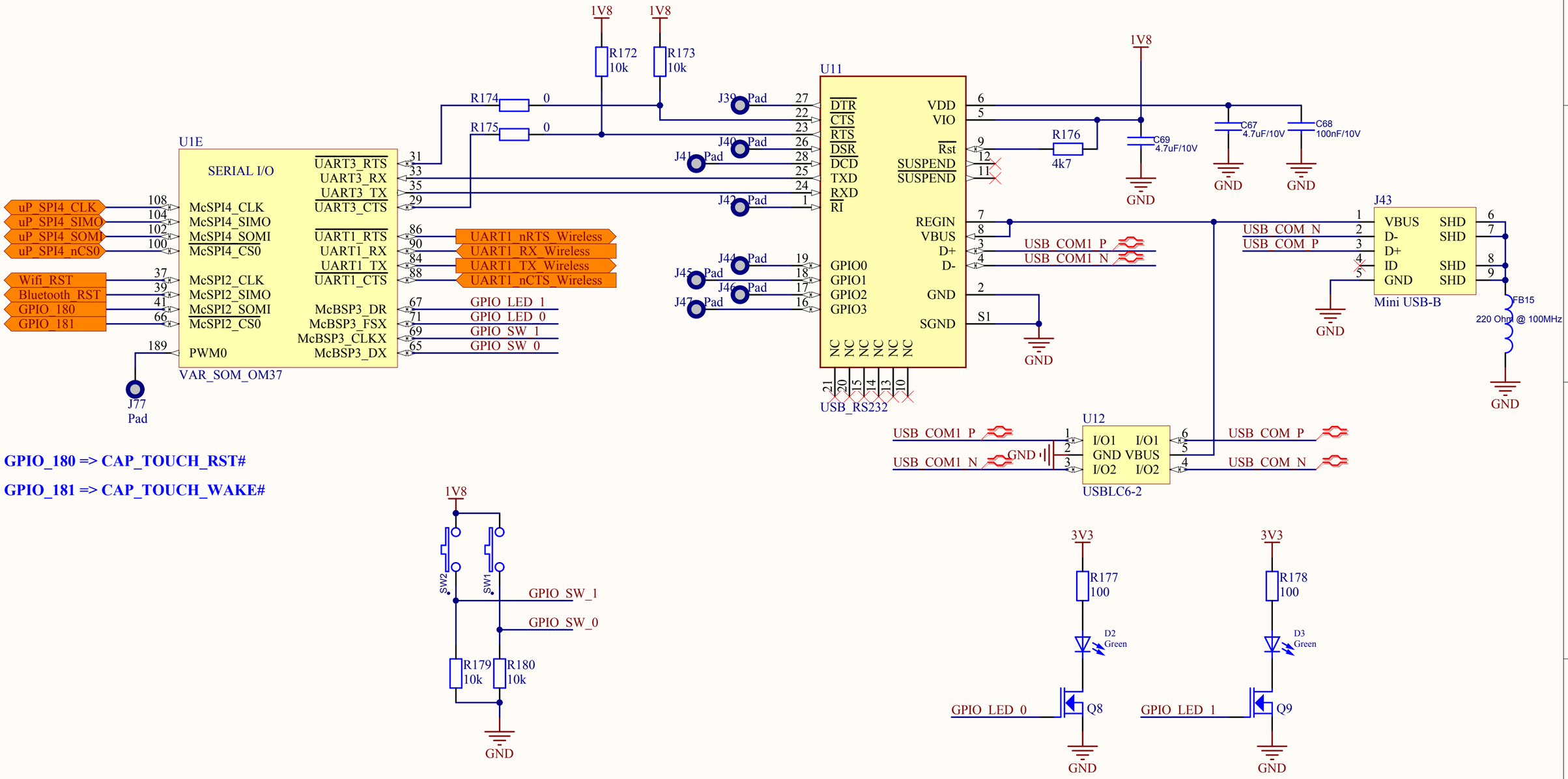
3G/GPS CONNECTION

Revision OK 03.10.2012 OAN/VTT

R&DS PCB_DM3730.PrjPCB	
DM3730_USB_PERIPHERAL.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 23 of 28

Correspondance SPI FPGA <=> CPU
SP6_SPI_SDO <=> up_SPI_SIMO (Slave In Master Out)
SP6_SPI_SDIO <=> up_SPI_SOMI (Slave Out Master In)

Revision OK 03.10.2012 OAN/VTT



GPIO_180 => CAP_TOUCH_RST#

GPIO_181 => CAP_TOUCH_WAKE#

RoDS PCB_DM3730.PrjPCB	
DM3730_SERIAL.SchDoc	Rev 0.5
Drawn by: ONH	Date: 10.10.2012
Approved by: *	Page 24 of 28

LAYOUT NOTE:

As close as possible to SODIMM connector

U1A

VIDEO

DSS_DATA0 DSS_DATA1 DSS_DATA2 DSS_DATA3 DSS_DATA4 DSS_DATA5 DSS_DATA6 DSS_DATA7 DSS_DATA8 DSS_DATA9 DSS_DATA10 DSS_DATA11 DSS_DATA12 DSS_DATA13 DSS_DATA14 DSS_DATA15 DSS_DATA16 DSS_DATA17 DSS_DATA18 DSS_DATA19 DSS_DATA20 DSS_DATA21 DSS_DATA22 DSS_DATA23

DSS_HSYNC DSS_PCLK DSS_VSYNC DSS_ACBIAS

TV_OUT

GPIO_28 GPIO_26

VAR_SOM_OM37

2	DSS_U1_D0	R22	22	DSS_D0
3	DSS_U1_D1	R23	22	DSS_D1
4	DSS_U1_D2	R25	22	DSS_D2
3	DSS_U1_D3	R27	22	DSS_D3
6	DSS_U1_D4	R29	22	DSS_D4
5	DSS_U1_D5	R31	22	DSS_D5
8	DSS_U1_D6	R34	22	DSS_D6
7	DSS_U1_D7	R36	22	DSS_D7
10	DSS_U1_D8	R38	22	DSS_D8
9	DSS_U1_D9	R39	22	DSS_D9
12	DSS_U1_D10	R40	22	DSS_D10
11	DSS_U1_D11	R42	22	DSS_D11
14	DSS_U1_D12	R44	22	DSS_D12
13	DSS_U1_D13	R46	22	DSS_D13
16	DSS_U1_D14	R48	22	DSS_D14
15	DSS_U1_D15	R50	22	DSS_D15
45	DSS_U1_D16	R52	22	DSS_D16
17	DSS_U1_D17	R53	22	DSS_D17
20	DSS_U1_D18	R54	22	DSS_D18
19	DSS_U1_D19	R56	22	DSS_D19
22	DSS_U1_D20	R58	22	DSS_D20
21	DSS_U1_D21	R60	22	DSS_D21
24	DSS_U1_D22	R62	22	DSS_D22
23	DSS_U1_D23	R64	22	DSS_D23
26	DSS_U1_HSYNC	R67	22	DSS_HSYNC
28	DSS_U1_PCLK	R69	22	DSS_PCLK
46	DSS_U1_VSYNC	R71	22	DSS_VSYNC
64	DSS_U1_ACBIAS	R73	22	DSS_ACBIAS
54	TV_OUT	J7 Pad		
109	GPIO_28 R77 22	LCD_BCKLT_EN		
19	GPIO_26	HDMI_PD		

LAYOUT NOTE:

BUS video des signaux DSS doivent tous être de la même longueur.

1V8 C25 4.7uF/10V C26 100nF/10V GND

3V3 C27 4.7uF/10V C28 100nF/10V GND

3V3 FB6 220 Ohm @ 100MHz 3V3_Display C29 4.7uF_10V C30 100nF/10V GND

5V FB7 220 Ohm @ 100MHz 5V_Display C31 4.7uF/10V C32 100nF/10V GND

U5 SN74AVC32T245

A5	1A1	1B1	DSS_U5_D2	R26 22 DSS_b_D2
A6	1A2	1B2	DSS_U5_D3	R28 22 DSS_b_D3
B5	1A3	1B3	DSS_U5_D4	R30 22 DSS_b_D4
B6	1A4	1B4	DSS_U5_D5	R32 22 DSS_b_D5
C5	1A5	1B5	DSS_U5_D6	R35 22 DSS_b_D6
C6	1A6	1B6	DSS_U5_D7	R37 22 DSS_b_D7
D5	1A7	1B7		
D6	1A8	1B8		
E5	2A1	2B1		
E6	2A2	2B2	DSS_U5_D10	R41 22 DSS_b_D10
F5	2A3	2B3	DSS_U5_D11	R43 22 DSS_b_D11
F6	2A4	2B4	DSS_U5_D12	R45 22 DSS_b_D12
G5	2A5	2B5	DSS_U5_D13	R47 22 DSS_b_D13
G6	2A6	2B6	DSS_U5_D14	R49 22 DSS_b_D14
H6	2A7	2B7	DSS_U5_D15	R51 22 DSS_b_D15
H5	2A8	2B8		
J5	3A1	3B1		
J6	3A2	3B2		
K5	3A3	3B3	DSS_U5_D18	R55 22 DSS_b_D18
K6	3A4	3B4	DSS_U5_D19	R57 22 DSS_b_D19
L5	3A5	3B5	DSS_U5_D20	R59 22 DSS_b_D20
L6	3A6	3B6	DSS_U5_D21	R61 22 DSS_b_D21
M5	3A7	3B7	DSS_U5_D22	R63 22 DSS_b_D22
M6	3A8	3B8	DSS_U5_D23	R65 22 DSS_b_D23
N5	4A1	4B1	DSS_U5_PCLK	R66 22 DSS_b_PCLK
N6	4A2	4B2	DSS_U5_HSYNC	R68 22 DSS_b_HSYNC
P5	4A3	4B3	DSS_U5_VSYNC	R70 22 DSS_b_VSYNC
P6	4A4	4B4	DSS_U5_ACBIAS	R72 22 DSS_b_ACBIAS
R5	4A5	4B5		
R6	4A6	4B6		
T6	4A7	4B7		
T5	4A8	4B8	T2	R74 22 LCD_BCKLT_EN_33
A3	1DIR	1OE	A4	
H3	2DIR	2OE	H4	
J3	3DIR	3OE	J4	
T3	4DIR	4OE	T4	

DSS_D2 DSS_D3 DSS_D4 DSS_D5 DSS_D6 DSS_D7 DSS_D10 DSS_D11 DSS_D12 DSS_D13 DSS_D14 DSS_D15 DSS_D18 DSS_D19 DSS_D20 DSS_D21 DSS_D22 DSS_D23 DSS_PCLK DSS_HSYNC DSS_VSYNC DSS_ACBIAS LCD_BCKLT_EN

LAYOUT NOTE:

As close as possible to level translator buffer

3V3_Display R24 DNP R33 1k GND

5V_Display J6

LCD_BCKLT_EN 33

3V3_Display

1	VLED		
2	VLED		
3	ADJ		
4	GLED		
5	GLED		
6	VCC		
7	VCC		
8	MODE		
9	DE	DSS_b_ACBIAS	
10	VS	DSS_b_VSYNC	
11	HS	DSS_b_HSYNC	
12	VSS		
13	LCD_B5	DSS_b_D7	
14	LCD_B4	DSS_b_D6	
15	LCD_B3	DSS_b_D5	
16	VSS		
17	LCD_B2	DSS_b_D4	
18	LCD_B1	DSS_b_D3	
19	LCD_B0	DSS_b_D2	
20	VSS		
21	LCD_G5	DSS_b_D15	
22	LCD_G4	DSS_b_D14	
23	LCD_G3	DSS_b_D13	
24	VSS		
25	LCD_G2	DSS_b_D12	
26	LCD_G1	DSS_b_D11	
27	LCD_G0	DSS_b_D10	
28	VSS		
29	LCD_R5	DSS_b_D23	
30	LCD_R4	DSS_b_D22	
31	LCD_R3	DSS_b_D21	
32	VSS		
33	LCD_R2	DSS_b_D20	
34	LCD_R1	DSS_b_D19	
35	LCD_R0	DSS_b_D18	
36	VSS		
37	DCLK	DSS_b_PCLK	
38	VSS		
39	L/R		
40	U/D		
41	SCH		
42	SCH		

40p FCC connector

3V3 R75 1k R76 DNP R78 DNP R79 1k GND

1V8 C39 100nF/10V C40 100nF/10V R80 0 R8 DNP

U7 TXS0102DCTR

3	VCCA	VCCB	7
5	A1	B1	8 TOUCH_CAP_I2C_SDA
4	A2	B2	1 TOUCH_CAP_I2C_SCL
6	OE	GND	2 GND

1V8 R85 4k7 R86 4k7

DM_I2C3_SCL DM_I2C3_SDA

3V3 1V8 R118 0 R81 DNP

1V8 C41 100nF/10V C42 100nF/10V GND

U8 TXS0102DCTR

3	VCCA	VCCB	7
5	A1	B1	8 TOUCH_CAP_INT
4	A2	B2	
6	OE	GND	2 GND

U1J

Touch control

I2C3_SDA I2C3_SCL I2C3_SCCBE

TSPX TSPY TSMX TSMY

VAR_SOM_OM37

61	DM_I2C3_SDA	
63	DM_I2C3_SCL	
62	GPIO_170	
73	TSPX	TSPX
75	TSPY	TSPY
77	TSMX	TSMX
79	TSMY	TSMY

C43 470pF/50V C44 470pF/50V C45 470pF/50V C46 470pF/50V GND GND GND GND

J12

TSMX 1 TSPY 2 TSPX 3 TSMY 4

MOLEX_52207-0485

3V3 1V8 R121 0 R137 DNP

1V8 C21 100nF/10V C22 100nF/10V GND

U4 TXS0102DCTR

3	VCCA	VCCB	7
5	A1	B1	8 TOUCH_CAP_RST
4	A2	B2	1 TOUCH_CAP_WAKE
6	OE	GND	2 GND

GPIO_180 GPIO_181

3V3 GND J11 Conn FCC 10pos

TOUCH_CAP_I2C_SCL TOUCH_CAP_I2C_SDA TOUCH_CAP_RST TOUCH_CAP_WAKE TOUCH_CAP_INT

1	VSS	
2	VDD	
3	SCL	TOUCH_CAP_I2C_SCL
4	NC	
5	SDA	TOUCH_CAP_I2C_SDA
6	NC	
7	RST	TOUCH_CAP_RST
8	WAKE	TOUCH_CAP_WAKE
9	INT	TOUCH_CAP_INT
10	VSS	
11	SCH	
12	SCH	

GND

12V R138 12 W5 1 2 Barette_2voies GND

Revision OK 03.10.2012 OAN/VTT

3V3 C35 4.7uF/10V C36 100nF/10V C37 4.7uF/10V C38 100nF/10V GND

U6 TFP410

DSS_D0	63	PD0	TX2-	30 HDMI2_N
DSS_D1	62	PD1	TX2+	31 HDMI2_P
DSS_D2	61	PD2		
DSS_D3	60	PD3		
DSS_D4	59	PD4		
DSS_D5	58	PD5		
DSS_D6	55	PD6		
DSS_D7	54	PD7		
DSS_D8	53	PD8	TX1-	27 HDMI1_N
DSS_D9	52	PD9	TX1+	28 HDMI1_P
DSS_D10	51	PD10		
DSS_D11	50	PD11		
DSS_D12	47	PD12		
DSS_D13	46	PD13		
DSS_D14	45	PD14		
DSS_D15	44	PD15		
DSS_D16	43	PD16		
DSS_D17	42	PD17		
DSS_D18	41	PD18		
DSS_D19	40	PD19		
DSS_D20	39	PD20		
DSS_D21	38	PD21		
DSS_D22	37	PD22		
DSS_D23	36	PD23		
DSS_PCLK	57	IDCK+		
	56	IDCK-		
DSS_ACBIAS	2	DE		
DSS_VSYNC	5	VSYNC		
DSS_HSYNC	4	HSYNC		
	3	VREF		
		PD		
		ISEL/RESET		
		BSEL/SCL		
		DSEL/SDA		
		DK3		
		DK2		
		DK1		
		EDGE/HTPLG		9 DSS_CLK_POLARITY
		TX0-		24 HDMI0_N
		TX0+		25 HDMI0_P
		TXC+		22 HDMIC_P
		TXC-		21 HDMIC_N
		TFADJ		19
		DKEN		35
		Reserved(Gnd)		34
		NC		49
		MSEN		11

DVDD DVDD DVDD PVDD TVDD TVDD — 12 33 18 23 29

DGND DGND DGND PGND TGND TGND TGND TH PAD — 48 64 17 20 26 32 65 16

3V3 R87 3k R93 1k GND

HDMI_PD

3V3 R94 10k R95 10k R97 10k R98 10k R99 1k R100 1k R101 1k

R92 510 R88 1k R89 1k R90 10k GND

3V3 R91 DNP DSS_CLK_POLARITY R96 10k GND

ASSEMBLY NOTE:
3.3V: DSS sampled at rising edge
GND: DSS sampled at falling edge

J8 HDMI_Conn

3	DAT2-		
1	DAT2+		
2	DAT2_S	SHLD	20
		SHLD	21
		SHLD	22
		SHLD	23
15	SCL		
16	SDA		
6	DAT1-		
4	DAT1+		
5	DAT1_S_SHLD		
18	+5V		
17	DDC/CEC		
9	DAT0-		
7	DAT0+		
8	DAT0_s		
11	CLK_S	CEC	13
10	CLK+	NC	14
12	CLK-	Hot_Plug	19

J9 Pad R82 DNP J10 Pad R83 DNP

5V R84 10

FB20 220 Ohm @ 100MHz

GND

Config SP6 (slave Serial connections)

CPU	SP3	SP6
GPIO_104	GPIO1P-----CCLK	CCLK
GPIO_96	GPIO1N-----DIN	DIN
GPIO_105	GPIO2P-----DONE	DONE
GPIO_94	GPIO3P-----INIT_B	INIT_B
GPIO_103	GPIO2N-----PROG_B	PROG_B

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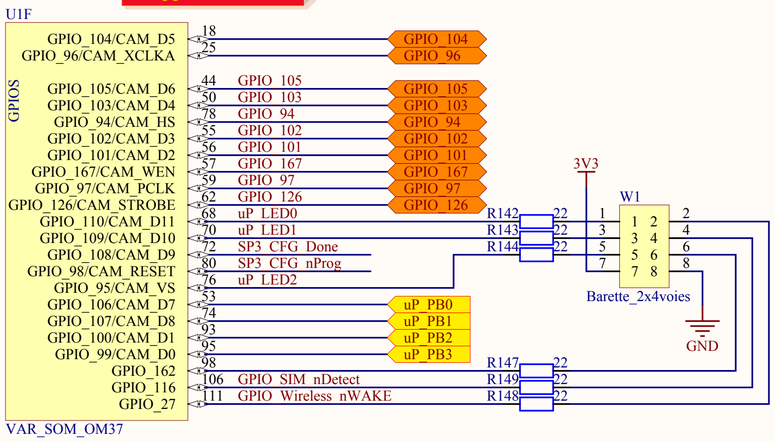
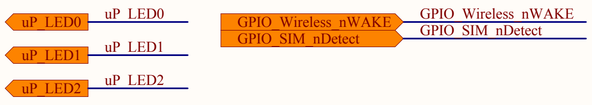
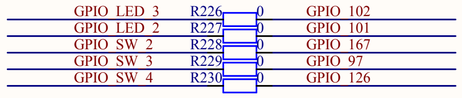
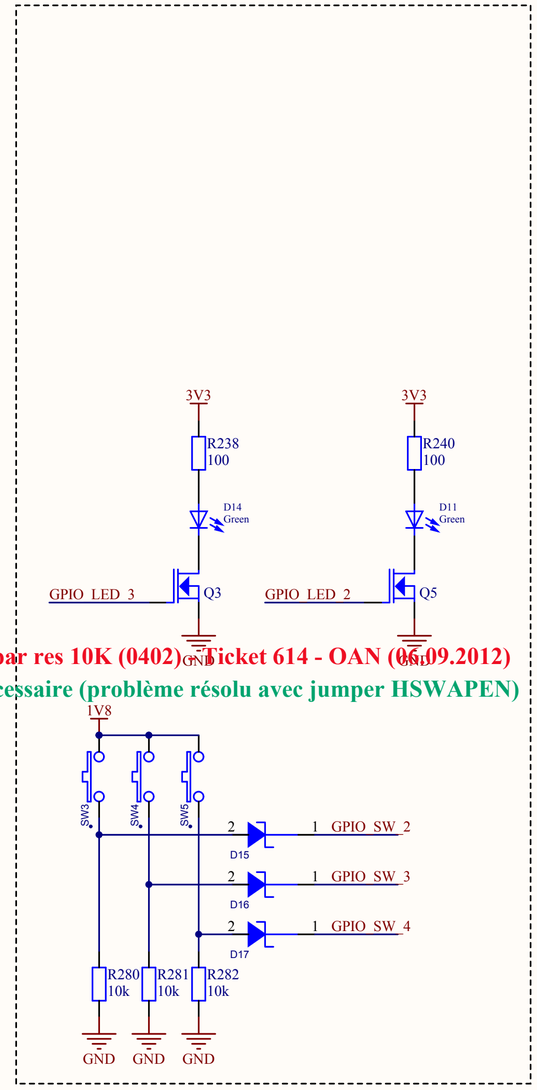
Tous les signaux de U1F peuvent être swapper entre eux.





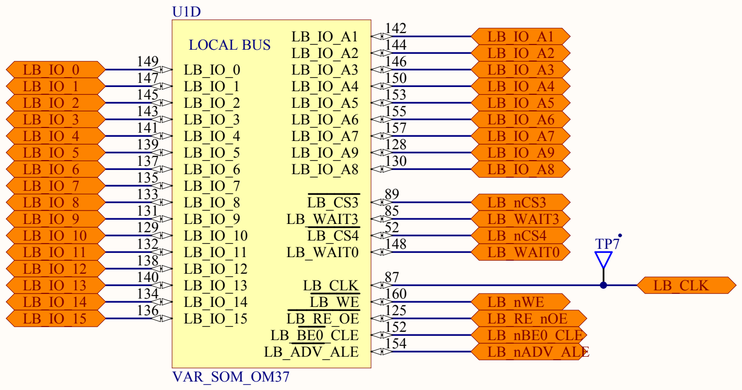
LED3 (GPIO_102) is common with CPU, SP3 and SP6
LED2, SW2, SW3, SW4 is common with CPU and SP6 only

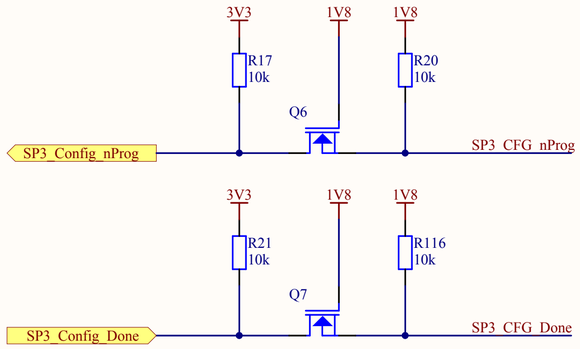




D15 à D17 à remplacer par res 10K (0402) - Ticket 614 - OAN (06.09.2012)

Ticket 614 - clos - 03.10.2012 - pas de modification nécessaire (problème résolu avec jumper HSWAPEN)





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DM3730_Local_Bus_GPIOS.SchDoc	Rev 0.5
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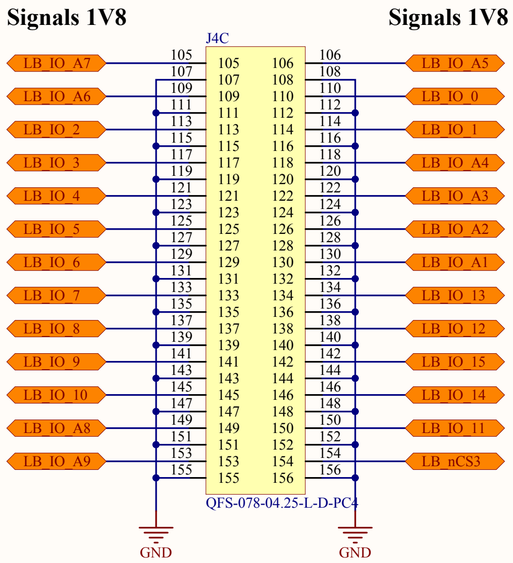
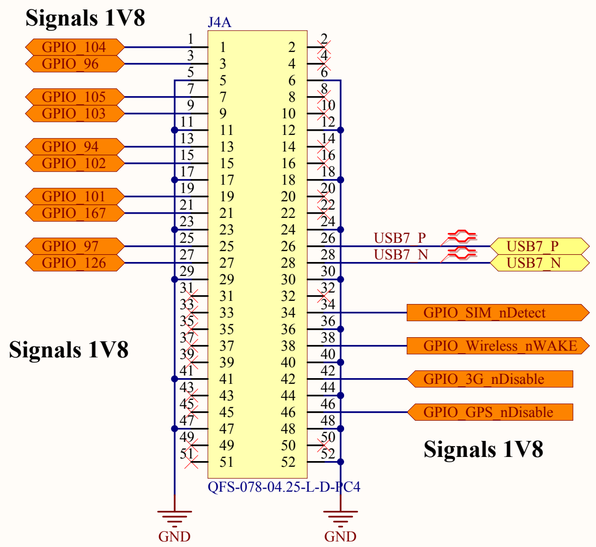
uP local bus



GPIOs GPS 3G



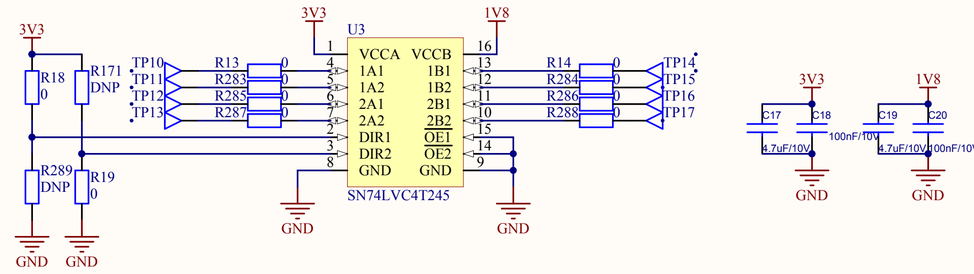
Layout note for QSH_60 pins and QFS-078-04.25-X-D-PC4 connectors

LAYOUT NOTE:

- Each differential pair should provide a differential impedance of 100ohm.
- Each single signal should provide an impedance of 50 ohm

uP GPIOS

Dir = 0 => B to A
Dir = 1 => A to B



Ne rien changer au pinout du connecteur car correspondance avec carte uP!!!

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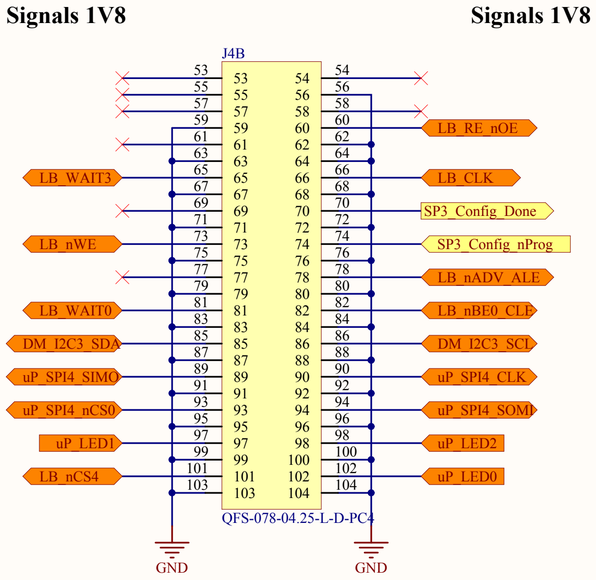
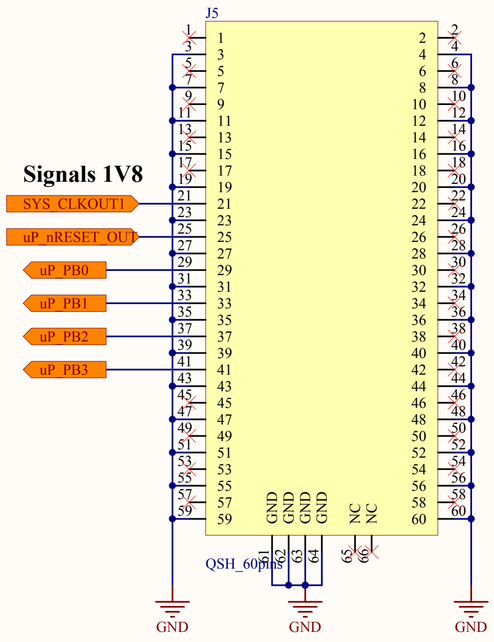
Config SP6 (slave Serial connections)

CPU	SP3	SP6
GPIO_104	GPIO1P-----CCLK	CCLK
GPIO_96	GPIO1N-----DIN	DIN
GPIO_105	GPIO2P-----DONE	DONE
GPIO_94	GPIO3P-----INIT_B	INIT_B
GPIO_103	GPIO2N-----PROG_B	PROG_B

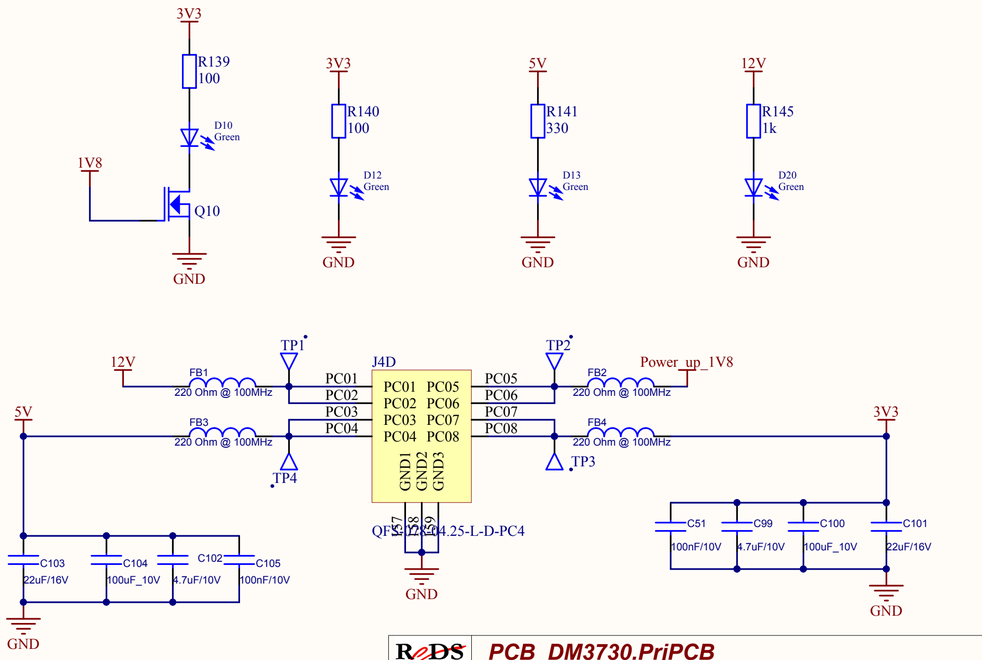
I2C UART uP_SWs uP_LEDs SPI



GPIOs SPI conf



POWER



R&DS **PCB_DM3730.PrjPCB**

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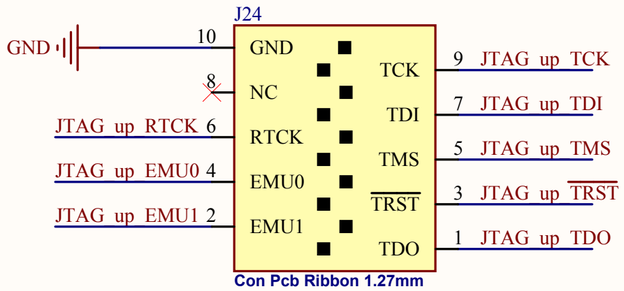
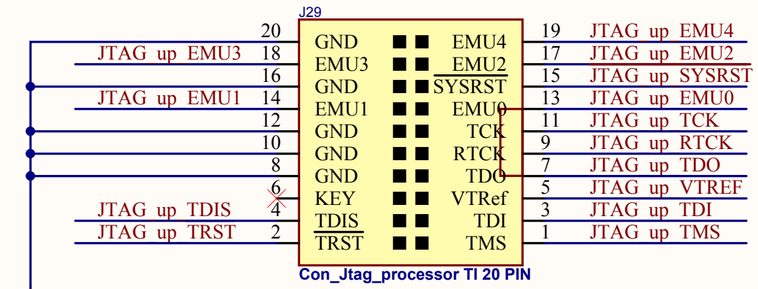
Barette pour carte processeur

Contre-connecteur pour carte processeur

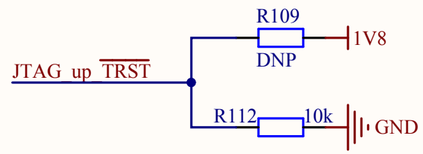
Connecteur Ribbon -> PCB FPGA



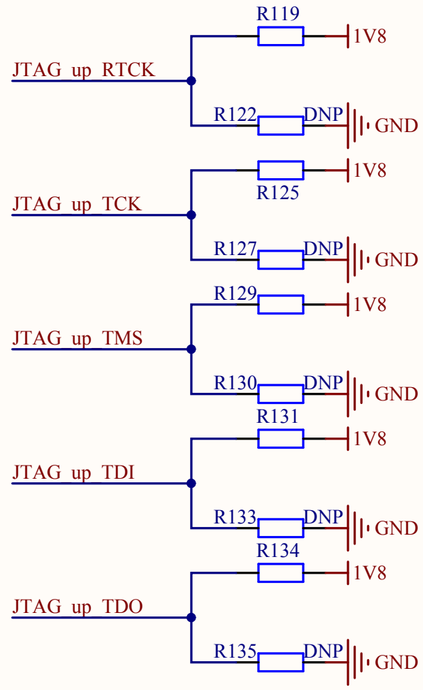


Ticket 601 - Détrompeur - Couper pin 6 sur carte CPU
A mettre dans rapport à Locatis (TODO)

Jtag shared signals Pull-Down

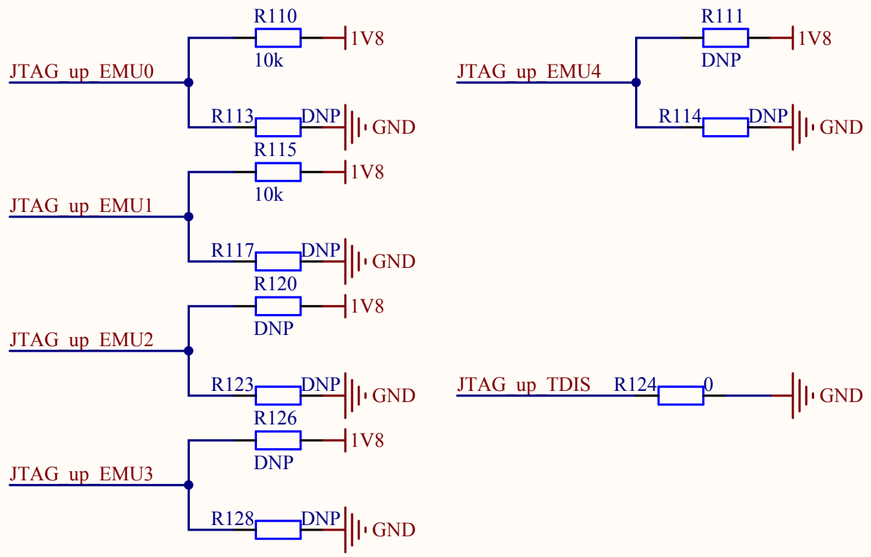


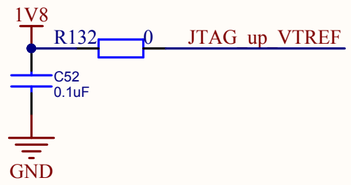
Jtag shared signals Pull-Up



Jtag shared signals

Jtag TI signals





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Con Jtag prog USB100V2

~~R~~e~~DS~~ PCB_DM3730.PrjPCB	
DM3730_JTAG.SchDoc	Rev *
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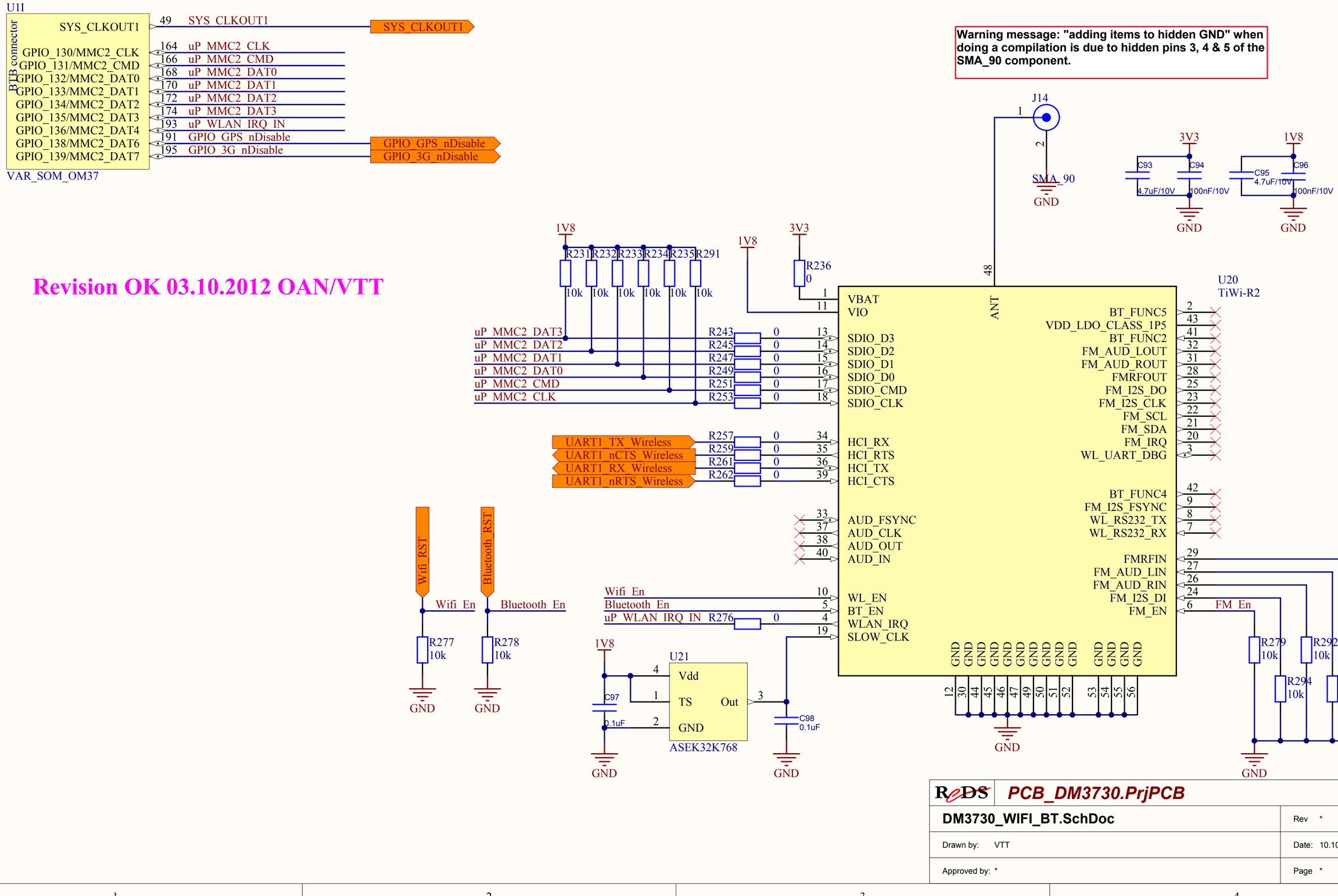
Approved by: *	Page * of *


U1I
BTB connector
SYS_CLKOUT1
GPIO_130/MMC2_CLK
GPIO_131/MMC2_CMD
GPIO_132/MMC2_DAT0
GPIO_133/MMC2_DAT1
GPIO_134/MMC2_DAT2
GPIO_135/MMC2_DAT3
GPIO_136/MMC2_DAT4
GPIO_138/MMC2_DAT6
GPIO_139/MMC2_DAT7
VAR_SOM_OM37
49 SYS_CLKOUT1
164 uP_MMC2_CLK
166 uP_MMC2_CMD
168 uP_MMC2_DAT0
170 uP_MMC2_DAT1
172 uP_MMC2_DAT2
174 uP_MMC2_DAT3
193 uP_WLAN_IRQ_IN
191 GPIO_GPS_nDisable
195 GPIO_3G_nDisable
SYS_CLKOUT1
GPIO_GPS_nDisable
GPIO_3G_nDisable
Warning message: "adding items to hidden GND" when doing a compilation is due to hidden pins 3, 4 & 5 of the SMA_90 component.
J14
SMA_90
GND
3V3
1V8
C93
C94
C95
C96
4.7uF/10V
100nF/10V
4.7uF/10V
100nF/10V
GND
GND
Revision OK 03.10.2012 OAN/VTT
1V8
R231 R232 R233 R234 R235 R291
10k 10k 10k 10k 10k 10k
3V3
1V8
R236
0
48
U20
TiWi-R2
VBAT
VIO
ANT
SDIO_D3
SDIO_D2
SDIO_D1
SDIO_D0
SDIO_CMD
SDIO_CLK
HCI_RX
HCI_RTS
HCI_TX
HCI_CTS
AUD_FSYNC
AUD_CLK
AUD_OUT
AUD_IN
WL_EN
BT_EN
WLAN_IRQ
SLOW_CLK
BT_FUNC5
VDD_LDO_CLASS_1P5
BT_FUNC2
FM_AUD_LOUT
FM_AUD_ROUT
FMRFOUT
FM_I2S_DO
FM_I2S_CLK
FM_SCL
FM_SDA
FM_IRQ
WL_UART_DBG
BT_FUNC4
FM_I2S_FSYNC
WL_RS232_TX
WL_RS232_RX
FMRFIN
FM_AUD_LIN
FM_AUD_RIN
FM_I2S_DI
FM_EN
GND
uP_MMC2_DAT3 R243 0 13
uP_MMC2_DAT2 R245 0 14
uP_MMC2_DAT1 R247 0 15
uP_MMC2_DAT0 R249 0 16
uP_MMC2_CMD R251 0 17
uP_MMC2_CLK R253 0 18
UART1_TX_Wireless R257 0 34
UART1_nCTS_Wireless R259 0 35
UART1_RX_Wireless R261 0 36
UART1_nRTS_Wireless R262 0 39
Wifi_RST
Bluetooth_RST
Wifi_En
Bluetooth_En
R277 10k
R278 10k
GND
GND
Wifi_En 10
Bluetooth_En 5
uP_WLAN_IRQ_IN R276 0 4
19
1V8
U21
Vdd
TS
Out
GND
C97
0.1uF
ASEK32K768
C98
0.1uF
GND
GND
FM_En
R279 10k
R292 10k
R293 10k
R294 10k
R295 10k
GND
R&DS
PCB_DM3730.PrjPCB
DM3730_WIFI_BT.SchDoc
Rev *
Drawn by: VTT
Date: 10.10.2012
Approved by: *
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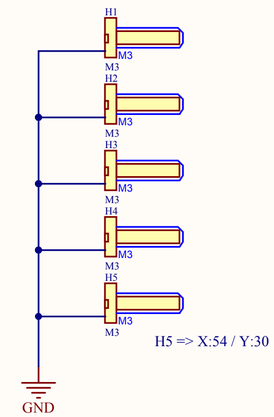

U_DM3730_ETHERNET
DM3730_ETHERNET.SchDoc

U_DM3730_USB_HUB
DM3730_USB_HUB.SchDoc

U_DM3730_AUDIO
DM3730_AUDIO.SchDoc

U_DM3730_SDCARD
DM3730_SDCARD.SchDoc

U_DM3730_JTAG
DM3730_JTAG.SchDoc

U23
uP_board_Production

U24
uP_PCB

U25
Touch screen

U26
Module VAR_SOM_OM37

U_DM3730_Local_Bus_GPIOS
DM3730_Local_Bus_GPIOS.SchDoc

GPIO_104 GPIO_96 GPIO_105 GPIO_103 GPIO_94 GPIO_102 GPIO_101 GPIO_167 GPIO_97 GPIO_126
SP3_Config_nProg SP3_Config_Done
GPIO_SIM_nDetect GPIO_Wireless_nWAKE
LB_nCS3 LB_WAIT3 LB_nCS4 LB_WAIT0 LB_nWE LB_RE_nOE LB_nBE0_CLE LB_nADV_ALE LB_CLK
LB_IO_A1 LB_IO_A2 LB_IO_A3 LB_IO_A4 LB_IO_A5 LB_IO_A6 LB_IO_A7 LB_IO_A8 LB_IO_A9
LB_IO_0 LB_IO_1 LB_IO_2 LB_IO_3 LB_IO_4 LB_IO_5 LB_IO_6 LB_IO_7 LB_IO_8 LB_IO_9 LB_IO_10 LB_IO_11 LB_IO_12 LB_IO_13 LB_IO_14 LB_IO_15
uP_PB0 uP_PB1 uP_PB2 uP_PB3
uP_LED0 uP_LED1 uP_LED2

U_DM3730_USB_PERIPHERAL
DM3730_USB_PERIPHERAL.SchDoc
USB7_P USB7_N

U_DM3730_POWER
DM3730_POWER.SchDoc
uP_nRESET_OUT

U_DM3730_SERIAL
DM3730_SERIAL.SchDoc
Wifi_RST Bluetooth_RST
GPIO_180 GPIO_181
uP_SPI4_nCS0 uP_SPI4_CLK uP_SPI4_SIMO uP_SPI4_SOMI
UART1_nRTS_Wireless UART1_RX_Wireless UART1_TX_Wireless UART1_nCTS_Wireless

U_DM3730_WIFI_BT
DM3730_WIFI_BT.SchDoc
UART1_nRTS_Wireless UART1_RX_Wireless UART1_TX_Wireless UART1_nCTS_Wireless
Wifi_RST Bluetooth_RST
GPIO_GPS_nDisable GPIO_3G_nDisable SYS_CLKOUT1

U_DM3730_Display
DM3730_Display.SchDoc
GPIO_180 GPIO_181
DM_I2C3_SDA DM_I2C3_SCL

U_DM3730_BTB_Conn
DM3730_BTB_Conn.SchDoc

SP3_Config_nProg SP3_Config_Done
GPIO_SIM_nDetect GPIO_Wireless_nWAKE
LB_nCS3 LB_WAIT3 LB_nCS4 LB_WAIT0 LB_nWE LB_RE_nOE LB_nBE0_CLE LB_nADV_ALE LB_CLK
LB_IO_A1 LB_IO_A2 LB_IO_A3 LB_IO_A4 LB_IO_A5 LB_IO_A6 LB_IO_A7 LB_IO_A8 LB_IO_A9
LB_IO_0 LB_IO_1 LB_IO_2 LB_IO_3 LB_IO_4 LB_IO_5 LB_IO_6 LB_IO_7 LB_IO_8 LB_IO_9 LB_IO_10 LB_IO_11 LB_IO_12 LB_IO_13 LB_IO_14 LB_IO_15
uP_PB0 uP_PB1 uP_PB2 uP_PB3
uP_LED0 uP_LED1 uP_LED2
GPIO_104 GPIO_96 GPIO_105 GPIO_103 GPIO_94 GPIO_102 GPIO_101 GPIO_167 GPIO_97 GPIO_126
USB7_P USB7_N
uP_nRESET_OUT
uP_SPI4_nCS0 uP_SPI4_CLK uP_SPI4_SIMO uP_SPI4_SOMI
GPIO_GPS_nDisable GPIO_3G_nDisable SYS_CLKOUT1
DM_I2C3_SCL DM_I2C3_SDA

TP5 TP6 TP18
GND GND GND

M9 M8 M7 M10 M5 M6 M1 M2 M3 M4
CibleBot CibleTop

Title		
Size A3	Number	Revision
Date: 10.10.2012		Sheet of
File: E:\GIT\..\uP_Board.SchDoc		Drawn By: