Spartan3 registers descriptions

Base address for SP3:
0x1A00_0000

VERSION1_REG	
Address	0x0000
Description	These two registers give the unique ID for each design FPGA
Reset	It depends on each design
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW version				ID FPGA			ID design FPGA								

Bits	Field name	Description	Type
15:12	HW version	Hardware version. A new number will be assigned to each new serial production. '0000': v1.0 (prototype 2, boards numbered 1 to 8) '0001': v1.1 (series 1, boards numbered 9 to 30) …….. : series x	R
11:9	ID FPGA	ID of the FPGA containing the design. A new number will be assigned to each FPGA of the expansion boards (FMC)'000': XC3S200AN-5FTG256C (Spartan 3 of REPTAR board) '001': XC6SLX150TFGG900-3 (Spartan 6 of REPTAR board) ……..: FPGA x of the board x	R
8:0	ID design FPGA	The**bits 8..6**indicate the design category: '000': basic design '001': internal project '010': demonstrator '011': teaching (laboratory/diploma) '100': external project '101': reserved '110': reserved '111': reserved (design under development when bits 5..0 are also '111111') The**bits 5..0**correspond to the unique ID assigned to each design, (see the REPTAR wiki on redmine) 'xxxxxxx': design x '1111111': design under development	R

VERSION2_REG	
Address	0x02
Description	These two registers give the unique ID for each design FPGA
Reset	It depends on each design
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID Sub-Design								Version number							

Bits	Field name	Description	Type
15:8	ID Sub-Design	The owner of each assigned ID design FPGA is responsible for manage the Sub-design ID and the Version number	R
8:0	Version number		R

CONSTANT_REG	
Address	0x04
Description	Read only register, used for Local Bus test
Reset	0x1234
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONSTANT															

Bits	Field name	Description	Type
15:0	CONSTANT	Constant 0x1234	R

LED_RED_REG	
Address	0x06
Description	This register control the state of the leds
Reset	0x0000
Type	W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										LED5	LED4	LED3	LED2	LED1	LED0

Bits	Field name	Description	Type
5:0	LEDx	State of the LED => active low	W
15:6	unassigned	read as '0'	-

LED_GREEN_REG	
Address	0x08
Description	This register control the state of the leds
Reset	0x0000
Type	W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										LED5	LED4	LED3	LED2	LED1	LED0

Bits	Field name	Description	Type
5:0	LEDx	State of the LED => active low	W
15:6	unassigned	read as '0'	-

DIP_SW_REG	
Address	0x0A
Description	This register contains the value of the dip switch and the push-buttons
Reset	0x0000
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				SW_PB1	SW_PB0	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1

FURTHEST RIGHT DIP SW

FURTHEST LEFT DIP SW

REM : changé numérotation des SW de 10 … 1 !!!!! EMI 2017 mars

Bits	Field name	Description	Type
15:12	unassigned	read as '0'	-
11:10	SW_PBx	Value of the push-button	R
9:1	SWx	Value of the dip switch	R

0	SW0	Value of the dip switch0: it must be always to '1' because is the local bus output enable	R

SP6_CONFIG_MODE_REG	
Address	0x0C
Description	This register select the configuration mode of the SP6
Reset	0x0000
Type	W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															CFGMODE

Bits	Field name	Description	Type
0	CFGMODE	when '0': the bitstream of the SP6 is loaded from the PlatformFlash when '1': the bitstream of the SP6 is loaded from the CPU	RW
15:1	unassigned	read as '0'	-

POWER_STATE_REG	
Address	0x0E
Description	Power chips indicator
Reset	0x0000
Type	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												PG12V	PG5V	PG3V3	PG2V5

Bits	Field name	Description	Type
0	PG2V5	Indication of PGOOD 2V5	R
1	PG3V3	Indication of PGOOD 3V3	R
2	PG5V	Indication of PGOOD 5V	R
3	PG12V	Indication of PGOOD 12V	R
15:4	unassigned	read as '0'	-

GPIO_3V3_REG	
Address	0x10
Description	This register controls the GPIOs 3V3, named "GPIO33_x" on the board silkscreen (header J38). These GPIOs are wired to SP6 GPIOs (see register SP6 with same name)
Reset	0x0000
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												GPIO4	GPIO3	GPIO2	GPIO1

!! GPIO5 plus disponible !!

Bits	Field name	Description	Type
3:0	GPIOx	GPIO value	RW
15:5	unassigned	read as '0'	-

GPIO_REG	**NOT USED**

Address	0x12
Description	This register control the GPIO connected with the CPU board and the SP6
Reset	0x0000
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										GPIO3P	GPIO3N	GPIO2P	GPIO2N	GPIO1P	GPIO1N

Bits	Field name	Description	Type
5:0	GPIOxx	GPIO value	RW
15:6	unassigned	read as '0'	-

GPIO_3V3_OE_REG

Address	0x14
Description	This register control the buffer tristate of the RW GPIOs
Reset	0x0000
Type	W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												GPIO_3V3_OE_4	GPIO_3V3_OE_3	GPIO_3V3_OE_2	GPIO_3V3_OE_1

Bits	Field name	Description	Type
3:0	GPIO_3V3_OE_x	bit = '0 => input / bit ='1' => output	RW
15:4	unassigned	read as '0'	-

Attention, si les GPIO sont en sortie sur SP3 les GPIO SP6 **DOIVENT** être en entrées ou vice versa !!!

SCRATCH1_REG

Address	0x16
Description	Read/Write register , used for Local Bus test
Reset	0x000000
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST															

Bits	Field name	Description	Type
15:0	TEST	Write a value and then check it by reading it back	RW

SCRATCH2_REG

Address	0x18
Description	Read/Write register , used for Local Bus test
Reset	0x000000
Type	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEST															

Bits	Field name	Description	Type
15:0	TEST	Write a value and then check it by reading it back	RW