Soft-Core Processors for Embedded Systems

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***Abstract*— A soft-core processor is a hardware description language (HDL) model of a specific processor (CPU) that can be customized for a given application and synthesized for an ASIC or FPGA target. In many applications, soft-core processors provide several advantages over custom designed processors such as reduced cost, flexibility, platform independence and greater immunity to obsolescence. Embedded systems are hardware and software components working together to perform a specific function. Usually they contain embedded processors that are often in the form of soft-core processors that execute software code. This paper presents a survey of soft-core processors that are used in embedded systems. Several soft-core processors available from commercial vendors and open-source communities are reviewed and compared based on major architectural features. In addition, several real world examples of embedded systems that employ soft-core processors are summarized. As the complexity of embedded systems continues to increase, it is expected that the usage of customizable soft-core processors will become more widespread.**

I. Introduction

Embedded Systems are hardware and software components working together to perform a specific application. They exist in abundance in our modern society and play a vital role in our everyday lives. They can be found in places such as our automobiles, in the medical field, in industrial control systems, and in entertainment electronics to name just a few [1]. The hardware platform of the embedded system often consists of a microprocessor, on-board memory, an output display, an input device for a user to enter data and application software. The design of embedded systems is now becoming increasingly difficult due to the tight constraints on area usage, size, power consumption and performance. In addition to these constraints, many embedded system developers are faced with tight time-to-market deadlines [2]. Hence, the hardware/software co-design methodology is often used to design embedded systems in order to help reduce the amount of time spent on development and debugging [3].

As the complexity of embedded systems designs increased over time, designing each and every hardware component of the system from scratch soon became far too impractical and expensive for most designers. Therefore, the idea of using pre-designed and pre-tested intellectual property (IP) cores in designs became an attractive alternative. Soft-core processors are microprocessors whose architecture and behaviour are fully described using a synthesizable subset of a hardware description language (HDL). They can be synthesized for any Application-Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA) technology, therefore they provide designers with a substantial amount of flexibility.

The use of soft-core processors holds many advantages for the designer of an embedded system. First, soft-core processors are flexible and can be customized for a specific application with relative ease. Second, since soft-core processors are technology independent and can be synthesized for any given target ASIC or FPGA technology, they are therefore more immune to becoming obsolete when compared with circuit or logic level descriptions of a processor. Finally, since a soft-core processor's architecture and behaviour are described at a higher abstraction level using an HDL, it becomes much easier to understand the overall design.

This paper presents a survey of the available soft-core processors that are used to design and implement embedded systems using either FPGAs or ASICs.

The organization of this paper is as follows: Section II provides a summary of available soft-core processors provided by major commercial vendors and open-source communities. Section III presents some applications which utilize soft-core processors. We compare several soft-core processors in Section IV based on important features such as the maximum clock rate, throughput, available cache memory, etc. We conclude in Section V with some comments on future work in the area of soft-core processors.

II. A Survey of Soft-Core Processors

In this section we will survey the available soft-core processors provided by commercial vendors and open source communities.

A. Commerical Cores and Tools

Nios II, MicroBlaze, PicoBlaze and Xtensa are the leading soft-core processors provided by Altera, Xilinx and Tensilica respectively. In this section, we will discuss the important features of each soft-core processor.

Nios II by Altera Corporation: Altera Corporation [4] is one of the leading vendors of Programmable Logic Devices (PLDs) and FPGAs. They offer the Stratix, Stratix II and Cyclone families of FPGAs that are widely used in the design of embedded systems and digital signal processing (DSP) applications. They also provide associated CAD tools such as Quartus II and System-on-Programmable-Chip (SOPC) Builder that allow designers to synthesize, program and debug their designs and build embedded systems on Altera's FPGAs.

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The Nios II Processor [5] is their flagship IP soft-core processor and can be instantiated with any embedded system design. This processor is the successor of Altera's original Nios soft-core processor and features major improvements focused on the reduction of logic element (LE) consumption on an FPGA and improved performance.

The Nios II Soft-Core Processor is a general purpose Reduced Instruction Set Computer (RISC) processor core and features a Harvard memory architecture. This core is widely used with Altera FPGAs and SOPC Builder. This processor features a full 32-bit Instruction Set Architecture (ISA), 32 general-purpose registers, single-instruction 32x32 multiply and divide operations, and dedicated instructions for 64-bit and 128-bit products of multiplication. The Nios II also has a performance of more than 150 Dhrystone MIPS (DMIPS) on the Stratix family of FPGAs. This soft-core processor comes in three versions: economy, standard and fast core. Each core version modifies the number of pipeline stages, instruction and data cache memories and hardware components for multiply and divide operations. In addition, each core varies in size and performance depending on the features that are selected. Adding peripherals with the Nios II Processors is done through the Avalon Interface Bus which contains the necessary logic to interface the processor with off-the-shelf IP cores or custom-made peripherals.

MicroBlaze and PicoBlaze by Xilinx Incorporated: Xilinx Incorporated [6] are the makers of the Spartan and Virtex families of FPGAs. In addition, they also offer soft IP cores that target their FPGAs. Their most popular and widely-used core is the MicroBlaze soft-core processor [7], which is a 32-bit processor that is optimized for embedded applications. It can operate at up to 200 MHz on a Virtex-4 FPGA, and it features a Harvard RISC architecture, 32-bit instructions, a 3-stage pipeline, a 32 register wide register file, a shift unit and two levels of interrupt. Memory can reside on-chip or as an external peripheral. On-chip memory can be accessed by MicroBlaze using a Local Memory Bus (LMB), which provides single-cycle access to the memory. Also, a general purpose interface known as the On-chip Peripheral Bus (OPB) can be used to interface MicroBlaze with both on-chip and off-chip memories as well as other peripherals.

The MicroBlaze processor includes a large set of configurable parameters that can be set at design time, including an optional IEEE-754 compatible single precision floating point unit (FPU), a hardware divider, a barrel shifter, data and instruction caches, exception handling capabilities, hardware debug logic, and some additional features. Designers are also provided with a low-latency interface to the MicroBlaze pipeline through the Fast Simplex Link (FSL) interface, which can include up to eight dedicated, 32-bit input and output ports. The FSL can be used to connect custom-designed hardware modules directly to the pipeline in order to accelerate time-critical tasks. The MicroBlaze soft-core processor is targeted for the Virtex and Spartan families of FPGAs only.

Xilinx also offers the Embedded Development Kit (EDK) which includes Xilinx Platform studio and a set of IP cores that are required for developing embedded systems using MicroBlaze. Xilinx also supplies the PicoBlaze soft-core processor [8], a compact 8-bit microcontroller that is optimized for the Spartan-3, Virtex-II and Virtex-II Pro families of FPGAs. The PicoBlaze processor is a small, cost-effective soft-core processor that is useful for simple data processing applications.

Diamond Standard Series and Xtensa by Tensilica Inc.: Tensilica Inc. [9] offers a number of soft IP processing cores for embedded systems design. Their Diamond Standard Series of synthesizable processors [10] offer a set of six pre-configured off-the-shelf processors with a variety of features. They range in size and feature set from small, power-optimized controllers such as the 108Mini RISC Controller, to large, high-performance cores such as the 545CK, which has been optimized for DSP applications. The Diamond Standard Series cores are currently available as synthesizable HDL descriptions of the processors written in Verilog [11].

Tensilica's flagship product is the Xtensa Series of "configurable and extensible" processors [12]. They are configurable in that they offer the designer a set of predefined parameters which they can configure in order to tailor the processor to the intended application. They are also extensible, in that designers can also invent custom instructions and execution units and integrate them directly into the processor core. The Xtensa processor is extended using the Tensilica Instruction Extension (TIE) language [13], which is a Verilog-like language that can be used to describe custom instructions. Designers can write TIE code manually and compile it using the TIE Compiler [14], or they can use the XPRES (Xtensa Processor Extension Synthesis) Compiler [15] to automatically create TIE descriptions of processor extensions. The XPRES Compiler can analyze a given algorithm written in C/C++ and automatically configure and extend the Xtensa processor so that it is optimized to run that particular algorithm. Finally, the Xtensa Processor Generator can be used to generate HDL descriptions of the customized processor, as well as a set of electronic design automation (EDA) scripts and a full suite of software development tools specifically suited for that processor design.

Tensilica currently offers two different versions of the Xtensa Processor: the Xtensa LX and the Xtensa 6. Both of these are configurable and extensible using TIE and the XPRES Compiler, but they each provide their own set of features and configurable options. The Xtensa LX is Tensilica's top-of-the-line product, and is optimized for high-performance DSP and other data intensive applications. By contrast, the Xtensa 6 is designed to optimize power consumption, and is well-suited to a wide variety of different applications.

B. Open-source Cores

Open-source cores are IP components that are freely available in the open-source community [16]. Usually these types of cores are used in academia for research as well in the development of embedded systems. UT Nios [17] is an example of an open-core processor used in academia. Sun Microsystems provides its own soft-core processor, OpenSPARC [18], which

is widely used in development of ASICs, but it can also be synthesized for FPGAs as well. In this section, we will review the LEON and OpenRISC 1200 soft-core processors that are available in the open-source community.

LEON by Gaisler Research: Gaisler Research [19] is a provider of IP cores and supporting development tools for embedded processors based on the SPARC architecture. Their main product is the LEON line of synthesizable soft-core processors and associated library of IP cores, called the GRLIB IP Library [21]. Several successive versions of the LEON processor have been developed, and currently Gaisler Research maintains and supplies the LEON2 and the LEON3 processors.

LEON2 [20] and LEON3 [21] are open-source VHDL models of a 32-bit processing core that is fully compliant with the standard IEEE-1754 SPARC V8 architecture. The cores come with SPARC V8 compliant integer units complete with hardware multiply, divide and MAC units. LEON2 features a 5-stage pipeline, while LEON3 has a pipeline depth of 7 stages. Both cores feature a Harvard memory architecture, and a configurable set-associative cache sub-system. The number of registers in their register files is configurable within the SPARC V8 standard (2 to 32 registers). LEON2 and LEON3 also provide an interface to one of several available floating point units (FPU) cores as well as custom co-processors. They also include support for an optional debug unit, timers, watchdogs, UARTs and interrupt controllers.

OpenRISC 1200: OpenRISC 1200 [16] is one of the popular open core processors available at OpenCores.org. This soft-core processor features a 32-bit and 64-bit RISC architecture suitable for numerous applications including networking and telecomm devices, home entertainment, consumer products, and automotive applications. This processor is optimized for high performance, low power consumption, and versatility in a wide range of applications.

The processor features a Harvard architecture containing separate data and instruction caches, each 8 KB in size. It has a 32-bit ISA containing the OpenRISC Basic Instruction Set (ORBIS32), a scalar, single-issue 5-stage pipeline delivering sustained throughput and single-cycle instruction execution on most instructions. The peak performance that it can provide is 250 DMIPS at a clock frequency of 250MHz. OpenRISC has the capability of expanding the instruction set architecture by adding additional components such as an FPU. Up to 8 units can be added to the core and controlled through registers or user defined custom instructions. This processor can be synthesized and downloaded onto Altera and Xilinx FPGAs and supports embedded real time operating systems such as Linux, μLinux and OAR RTEMS real time operating system. For software development, tools are available that allow developers to compile programs written in C/C++, Java and Fortran to run on the OpenRISC processor.

III. Some Example Applications

In this section, we discuss some practical applications that utilize a few of the soft-core processors discussed above.

A. Communciations

Broadcom [22] has chosen to use the Tensilica Xtensa processor in the BCM1500 Project [23], whose goal was to design a class of flexible and reconfigurable access communication components for broadband communication and voice, video and data networking. Five Xtensa processors were deployed as control processors in their CALISTO^{TM} architecture, which manages computationally intensive data processing tasks such as "echo cancellation, data modem signal processing and delay equalization, and protocols for packet telephony applications." [23]

Cisco Systems' new Cisco Carrier Routing System (CRS-1) utilizes 192 Xtensa configurable cores in their Cisco Silicon Packet Processor [24]. The CRS-1 system is unique in the industry, in that it is the only carrier routing system that scales up to 92 terabits per second. The CRS-1 system has enough capacity to run an 850 kilobit-per-second line to every house in the United States.

B. Advertising

Advanced Electronic Designs, Inc. (AED) [25] designed an LED sign for JPMorgan Chase^{TM} in Times Square in New York City using Xilinx components [26]. The sign they designed is 135 feet in length and 26 feet high and has a resolution of nearly two million pixels, making it the highest resolution sign in the world. For the design, AED utilized Xilinx Virtex-II and Spartan-3 FPGAs and over 1,000 PicoBlaze processors. The processors were used for control functions and for testing and debugging purposes. One of the major applications of the PicoBlaze processors in this project was in the Ethernet controllers that are responsible for sending data to different parts of the sign. They also made the testing and debugging process easier, since making changes to their control functions simply involved changing the program code stored in their block RAM.

C. Security and Authentication

Seven graduate students and their advisor at the University of California, Los Angeles (UCLA) used the LEON2 soft-core processor in their architecture for the ThumbPod [27], an FPGA-based prototype for a fingerprint authentication device. In the prototype, the LEON2 processor is configured onto a Xilinx Virtex-II FPGA along with two co-processors: an encryption processor implementing the Advanced Encryption Standard (AES) and a Discrete Fourier Transform (DFT) processor. The LEON2 processor serves as the main core processor of the device and runs an embedded Java kilobyte virtual machine (KVM) to aid in software development. The ThumbPod is able to capture a fingerprint, extract its features, compare it to a known template, and return a matching score from 0 to 100 indicating the degree to which the captured fingerprint matches the template.

IV. Comparison of Soft-core Processors

Table I below shows a comparison of the features and characteristics of several processors that we have surveyed.

TABLE I
COMPARISON OF SOFT-CORE PROCESSORS

Category	Nios II (Fast Core)	MicroBlaze	Xtensa XL	OpenRISC 1200	LEON3
Maximum MHz	200 (FPGA)	200 (FPGA)	350 (ASIC)	300 (ASIC)	400/125 (ASIC/FPGA)
ASIC/FPGA Technology	– /Stratix and Stratix II	– /Virtex-4	0.13 μm/ –	0.18 μm/ –	0.13 μm/Not given
Reported DMIPS	150 DMIPs	166 DMIPs	–	250 DMIPS	85 DMIPs
ISA	32-bit RISC	32-Bit RISC	32-Bit RISC	32-bit RISC	32 or 64-bit RISC
Cache Memory (I/D)	Up to 64 KB	Up to 64 KB	Up to 32 KB (1)	Up to 64 KB	Up to 256 KB
Floating Point Unit (optional)	IEEE-754	IEEE-754	IEEE-754	As peripheral	IEEE-754
Pipeline	6 Stages	3 Stages	5 Stages	5 Stages	7 Stages
Custom Instructions	Up to 256 Instructions	None	Unlimited	Unspecified limit	None
Register File Size	32	32	32 or 64	32	2 to 32
Implementation	FPGA	FPGA	FPGA, ASIC	FPGA, ASIC	FPGA, ASIC
Area	700-1800 LEs	1269 LUTs	0.26 mm^2	N/A	N/A

(1) Using 1, 2 or 4-way set associative configuration.

The first column presents the features across which the processors are being compared. The subsequent columns show the available features inside of each soft-core processor.

As shown in the table, LEON3 has the highest operating frequency for ASIC implementation but has the lowest for FPGA implementation. The Nios II and Microblaze soft-core processors have the highest operating frequency for FPGA implementation. However, frequencies for ASIC implementation are not mentioned.

All soft-core processors have optional floating point units which are either included in their architecture or instantiated as a peripheral connected to the core.

Xtensa XL is the most flexible core out of all that are listed in the table. This is due to the fact that designers can create a limitless number of custom instructions and execution units using the TIE language and integrate them directly into the processor's core. In addition, Xtensa also features a large number of configurable parameters that the designer can choose from. Nios II also has the capability of expanding its instruction set by adding up to 256 custom instructions. MicroBlaze does not have this kind of feature.

Nios II and Microblaze soft-core processors are targeted and optimized mainly for FPGA implementation. In contrast, the other three cores are not optimized for any specific target technology.

Each core surveyed has different performance characteristics and features that are suitable for specific applications. Embedded system designers should choose a processor core based on the requirements and performance constraints of their particular application.

V. CONCLUSION AND FUTURE WORK

In this paper we have surveyed a number of soft-core processors that are used in industrial and research applications. The increasing popularity of soft-core processors will inevitably lead to more widespread usage in embedded system design. This is due to a number of significant advantages that soft-core processors hold over circuit or logic-level processor descriptions.

Currently, we are working on developing a Computer Aided Design (CAD) tool that will enable designers to rapidly construct soft-core processors and to explore various architectural tradeoffs. Our goal is to further advance our knowledge of the design and implementation of soft-core processors targeting FPGA technologies.

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